# MO2018
## High Temp, Single-Chip, SOT23 Oscillator

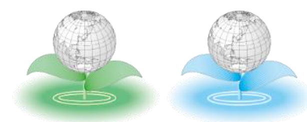
KDS DAISHINKU CORP.

### Features

- Frequencies between 1 MHz and 110 MHz accurate to 6 decimal places
- Operating temperature from -40°C to +125°C. For -55°C option, refer to MO2020 and MO2021
- Supply voltage of +1.8V or +2.5V to +3.3V
- Excellent total frequency stability as low as ±20ppm
- Low power consumption of +3.5mA typical at 20 MHz, +1.8V
- LVCMOS/LVTTL compatible output
- 5-pin SOT23-5 package: 2.9mm x 2.8mm
- RoHS and REACH compliant, Pb-free, Halogen-free and Antimony-free
- For AEC-Q100 clock generators, refer to MO2024 and MO2025

### Applications

- Industrial, medical, automotive, avionics and other high temperature applications
- Industrial sensors, PLC, motor servo, outdoor networking equipment, medical video cam, asset tracking systems, etc.




## Electrical Specifications

### Table 1. Electrical Characteristics

All Min and Max limits are specified over temperature and rated operating voltage with 15 pF output load unless otherwise stated. Typical values are at +25°C and nominal supply voltage.

| Parameters | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| **Frequency Range** | | | | | | |
| **Output Frequency Range** | f | 1.0 | – | 110 | MHz | Refer to Table 14 for the exact list of supported frequencies list of supported frequencies |
| **Frequency Stability and Aging** | | | | | | |
| **Frequency Stability** | F_stab | -20 | – | +20 | ppm | Inclusive of Initial tolerance at +25°C, 1st year aging at +25°C, and variations over operating temperature, rated power supply voltage and load (15 pF ± 10%). |
| | | -25 | – | +25 | ppm | |
| | | -30 | – | +30 | ppm | |
| | | -50 | – | +50 | ppm | |
| **Operating Temperature Range** | | | | | | |
| **Operating Temperature Range (ambient)** | T_use | -40 | – | +105 | °C | Extended Industrial |
| | | -40 | – | +125 | °C | Automotive |
| **Supply Voltage and Current Consumption** | | | | | | |
| **Supply Voltage** | Vdd | +1.62 | +1.8 | +1.98 | V | |
| | | +2.25 | +2.5 | +2.75 | V | |
| | | +2.52 | +2.8 | +3.08 | V | |
| | | +2.7 | +3.0 | +3.3 | V | |
| | | +2.97 | +3.3 | +3.63 | V | |
| | | +2.25 | – | +3.63 | V | |
| **Current Consumption** | Idd | – | +3.8 | +4.7 | mA | No load condition, f = 20 MHz, Vdd = +2.8V, +3.0V or +3.3V |
| | | – | +3.6 | +4.5 | mA | No load condition, f = 20 MHz, Vdd = +2.5V |
| | | – | +3.5 | +4.5 | mA | No load condition, f = 20 MHz, Vdd = +1.8V |
| **OE Disable Current** | I_od | – | – | +4.5 | mA | Vdd = +2.5V to +3.3V, OE = Low, Output in high Z state. |
| | | – | – | +4.3 | mA | Vdd = +1.8V, OE = Low, Output in high Z state. |
| **Standby Current** | I_std | – | +2.6 | +8.5 | µA | Vdd = +2.8V to +3.3V, $\overline{ST}$ = Low, Output is weakly pulled down |
| | | – | +1.4 | +5.5 | µA | Vdd = +2.5V, $\overline{ST}$ = Low, Output is weakly pulled down |
| | | – | +0.6 | +4.0 | µA | Vdd = +1.8V, $\overline{ST}$ = Low, Output is weakly pulled down |
| **LVCMOS Output Characteristics** | | | | | | |
| **Duty Cycle** | DC | 45 | – | 55 | % | All Vdds |
| **Rise/Fall Time** | Tr, Tf | – | 1.0 | 2.0 | ns | Vdd = +2.5V, +2.8V, +3.0V or +3.3V, 20% - 80% |
| | | – | 1.3 | 2.5 | ns | Vdd =+1.8V, 20% - 80% |
| | | – | 1.0 | 3.0 | ns | Vdd = +2.25V - +3.63V, 20% - 80% |
| **Output High Voltage** | VOH | 90% | – | – | Vdd | IOH = -4.0 mA (Vdd = +3.0V or +3.3V)<br>IOH = -3.0 mA (Vdd = +2.8V or +2.5V)<br>IOH = -2.0 mA (Vdd = +1.8V) |
| **Output Low Voltage** | VOL | – | – | 10% | Vdd | IOL = +4.0 mA (Vdd = +3.0V or +3.3V)<br>IOL = +3.0 mA (Vdd = +2.8V or +2.5V)<br>IOL = +2.0 mA (Vdd = +1.8V) |

### Table 1. Electrical Characteristics (continued)

| Parameters | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| **Input Characteristics** | | | | | | |
| **Input High Voltage** | VIH | 70% | – | – | Vdd | Pin 3, OE or $\overline{ST}$ |
| **Input Low Voltage** | VIL | – | – | 30% | Vdd | Pin 3, OE or $\overline{ST}$ |
| **Input Pull-up Impedence** | Z_in | 50 | 87 | 150 | kΩ | Pin 3, OE logic high or logic low, or $\overline{ST}$ logic high |
| | | 2.0 | – | – | MΩ | Pin 3, $\overline{ST}$ logic low |
| **Startup and Resume Timing** | | | | | | |
| **Startup Time** | T_start | – | – | 5.0 | ms | Measured from the time Vdd reaches its rated minimum value |
| **Enable/Disable Time** | T_oe | – | – | 130 | ns | f = 110 MHz. For other frequencies, T_oe = 100 ns + 3 * clock periods |
| **Resume Time** | T_resume | – | – | 5.0 | ms | Measured from the time $\overline{ST}$ pin crosses 50% threshold |
| **Jitter** | | | | | | |
| **RMS Period Jitter** | T_jitt | – | 1.6 | 2.5 | ps | f = 75 MHz, Vdd = +2.5V, +2.8V, +3.0V or +3.3V |
| | | – | 1.9 | 3.0 | ps | f = 75 MHz, Vdd = +1.8V |
| **Peak-to-peak Period Jitter** | T_pk | – | 12 | 20 | ps | f = 75 MHz, Vdd = +2.5V, +2.8V, +3.0V or +3.3V |
| | | – | 14 | 25 | ps | f = 75 MHz, Vdd = +1.8V |
| **RMS Phase Jitter (random)** | T_phj | – | 0.5 | 0.8 | ps | f = 75 MHz, Integration bandwidth = 900 kHz to 7.5 MHz |
| | | – | 1.3 | 2.0 | ps | f = 75 MHz, Integration bandwidth = 12 kHz to 20 MHz |

### Table 2. Pin Description

| Pin | Symbol | Functionality | |
|---|---|---|---|
| 1 | GND | Power | Electrical ground |
| 2 | NC | No Connect | No connect |
| 3 | OE/ $\overline{ST}$/NC | Output Enable | H[1]: specified frequency output<br>L: output is high impedance. Only output driver is disabled. |
| | | Standby | H or Open[1]: specified frequency output<br>L: output is low (weak pull down). Device goes to sleep mode. Supply current reduces to I_std. |
| | | No Connect | Any voltage between 0 and Vdd or Open[1]: Specified frequency output. Pin 3 has no function. |
| 4 | VDD | Power | Power supply voltage[2] |
| 5 | OUT | Output | Oscillator output |

**Notes:**

1. In OE or $\overline{ST}$ mode, a pull-up resistor of 10 kΩ or less is recommended if pin 3 is not externally driven. If pin 3 needs to be left floating, use the NC option.
2. A capacitor of value 0.1 µF or higher between Vdd and GND is required.

**Top View**

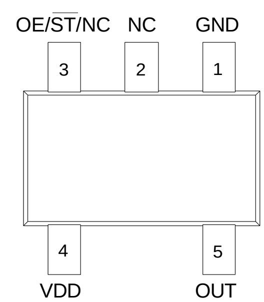



**Figure 1. Pin Assignments**

## Table 3. Absolute Maximum Limits

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

| Parameter | Min. | Max. | Unit |
|---|---|---|---|
| **Storage Temperature** | -65 | +150 | °C |
| **Vdd** | -0.5 | +4.0 | V |
| **Electrostatic Discharge** | – | +2000 | V |
| **Soldering Temperature (follow standard Pb free soldering guidelines)** | – | +260 | °C |
| **Junction Temperature[3]** | – | +150 | °C |

**Note:**

3. Exceeding this temperature for extended period of time may damage the device.

## Table 4. Thermal Consideration[4]

| Package | $\theta_{JA}$, 4 Layer Board (°C/W) | $\theta_{JC}$, Bottom (°C/W) |
|---|---|---|
| **SOT23-5** | 421 | 175 |

**Note:**

4. Refer to JESD51 for $\theta_{JA}$ and $\theta_{JC}$ definitions, and reference layout used to determine the $\theta_{JA}$ and $\theta_{JC}$ values in the above table.

## Table 5. Maximum Operating Junction Temperature[5]

| Max Operating Temperature (ambient) | Maximum Operating Junction Temperature |
|---|---|
| +105°C | +115°C |
| +125°C | +135°C |

**Note:**

5. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

## Table 6. Environmental Compliance

| Parameter | Condition/Test Method |
|---|---|
| **Mechanical Shock** | **MIL-STD-883F, Method 2002** |
| **Mechanical Vibration** | **MIL-STD-883F, Method 2007** |
| **Temperature Cycle** | **JESD22, Method A104** |
| **Solderability** | **MIL-STD-883F, Method 2003** |
| **Moisture Sensitivity Level** | **MSL1 @ 260°C** |

## Test Circuit and Waveform[6]

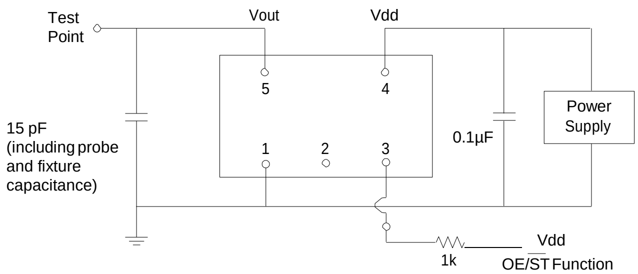



**Figure 2. Test Circuit**

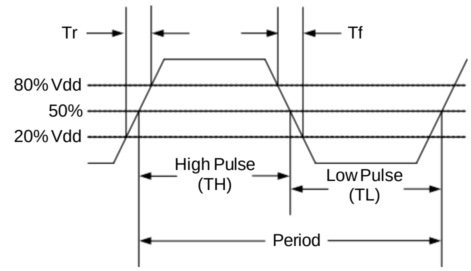
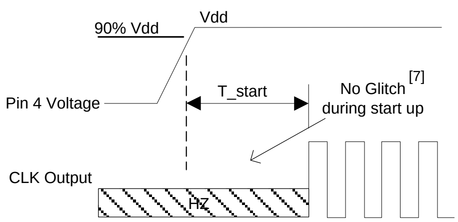



**Figure 3. Output Waveform**

**Note:**

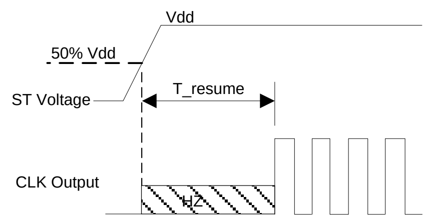
6. Duty Cycle is computed as Duty Cycle = TH/Period.

## Timing Diagrams



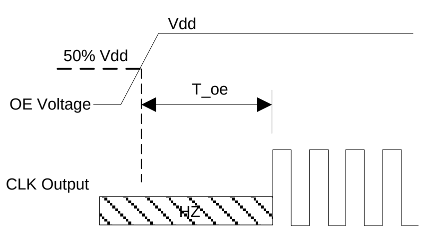

T_start: Time to start from power-off

**Figure 4. Startup Timing (OE/ST Mode)**



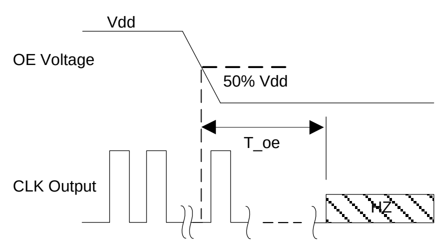

T_resume: Time to resume from ST

**Figure 5. Standby Resume Timing (ST Mode Only)**




T_oe: Time to re-enable the clock output

**Figure 6. OE Enable Timing (OE Mode Only)**




T_oe: Time to put the output in High Z mode

**Figure 7. OE Disable Timing (OE Mode Only)**

**Note:**

7. MO2018 has “no runt” pulses and “no glitch” output during startup or resume.

## Performance Plots[8]

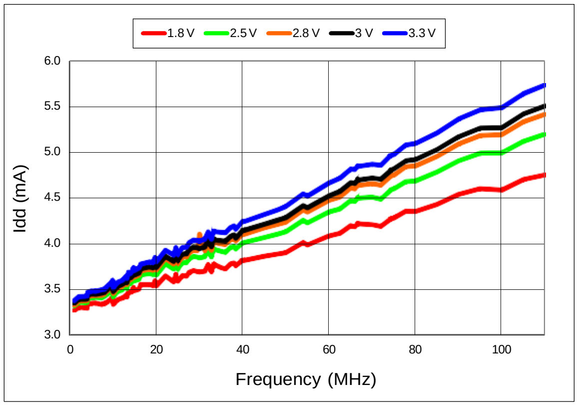



**Figure 8. Idd vs Frequency**

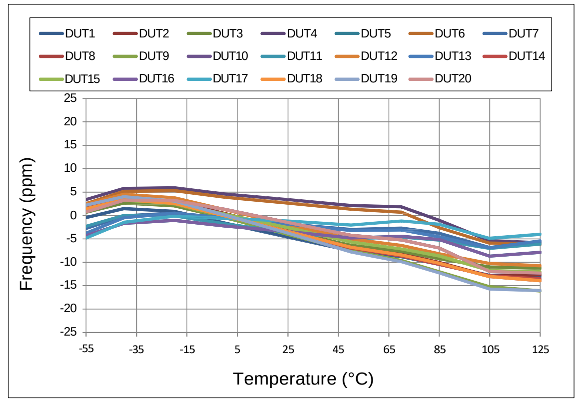



**Figure 9. Frequency vs Temperature**

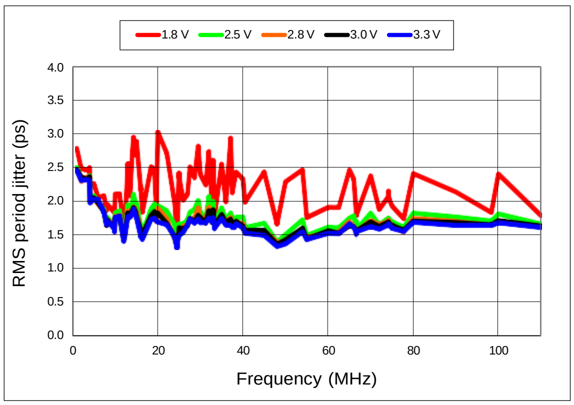



**Figure 10. RMS Period Jitter vs Frequency**

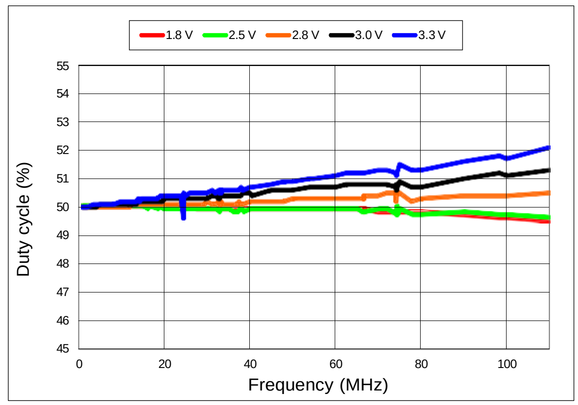



**Figure 11. Duty Cycle vs Frequency**

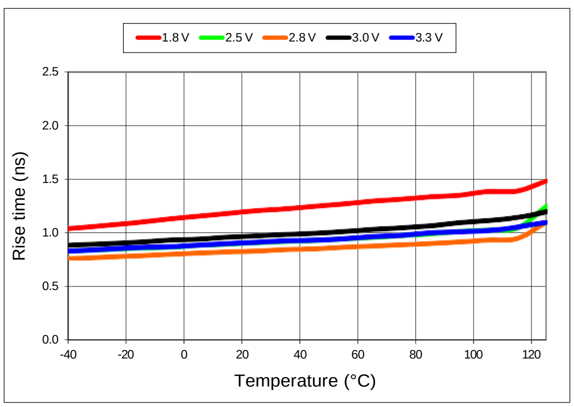



**Figure 12. 20%-80% Rise Time vs Temperature**

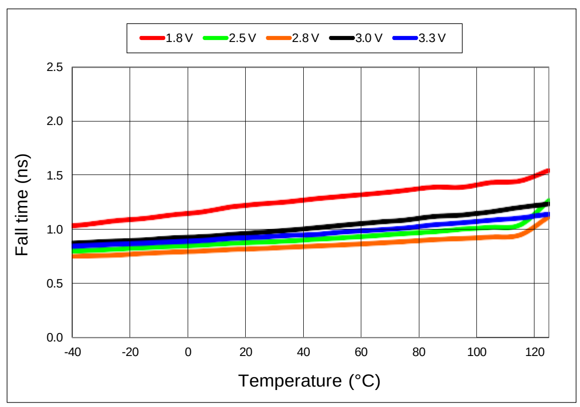



**Figure 13. 20%-80% Fall Time vs Temperature**

## Performance Plots[8]

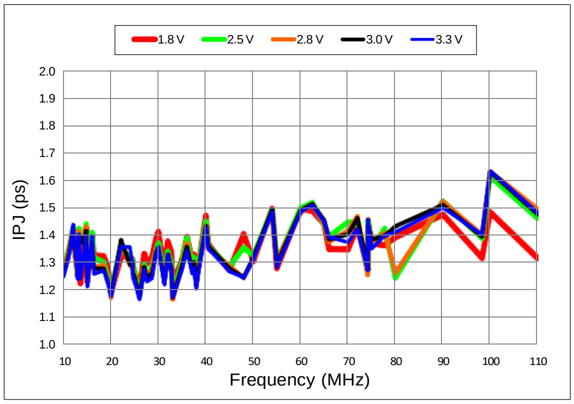



**Figure 14. RMS Integrated Phase Jitter Random (12k to 20 MHz) vs Frequency[9]**

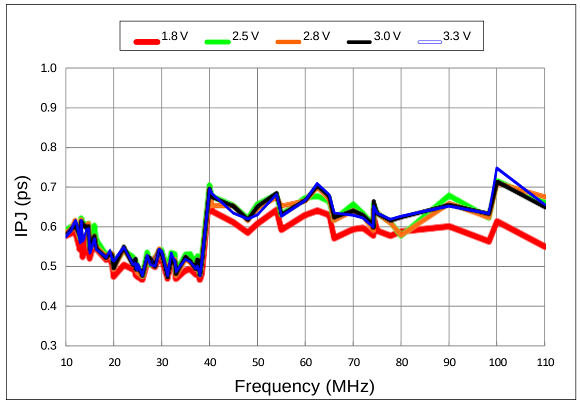



**Figure 15. RMS Integrated Phase Jitter Random (900 kHz to 20 MHz) vs Frequency[9]**

**Notes:**

8. All plots are measured with 15 pF load at room temperature, unless otherwise stated.
9. Phase noise plots are measured with Agilent E5052B signal source analyzer. Integration range is up to 5 MHz for carrier frequencies up to 40 MHz.

## Programmable Drive Strength

The MO2018 includes a programmable drive strength feature to provide a simple, flexible tool to optimize the clock rise/fall time for specific applications. Benefits from the programmable drive strength feature are:

- Improves system radiated electromagnetic interference (EMI) by slowing down the clock rise/fall time
- Improves the downstream clock receiver's (RX) jitter by decreasing (speeding up) the clock rise/fall time.
- Ability to drive large capacitive loads while maintaining full swing with sharp edge rates.

For more detailed information about rise/fall time control and drive strength selection, contact KDS.

### EMI Reduction by Slowing Rise/Fall Time

Figure 16 shows the harmonic power reduction as the rise/fall times are increased (slowed down). The rise/fall times are expressed as a ratio of the clock period. For the ratio of 0.05, the signal is very close to a square wave. For the ratio of 0.45, the rise/fall times are very close to near-triangular waveform. These results, for example, show that the 11th clock harmonic can be reduced by 35 dB if the rise/fall edge is increased from 5% of the period to 45% of the period.

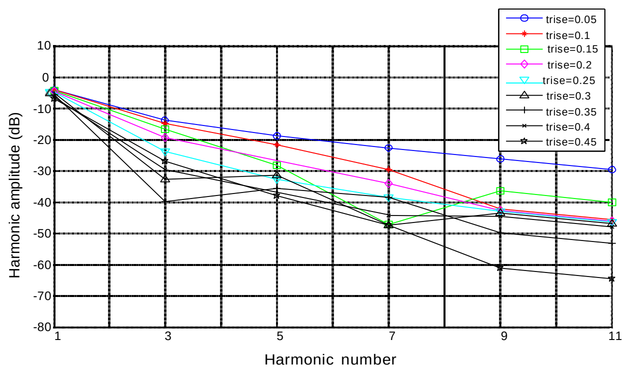



**Figure 16. Harmonic EMI reduction as a Function of Slower Rise/Fall Time**

### Jitter Reduction with Faster Rise/Fall Time

Power supply noise can be a source of jitter for the downstream chipset. One way to reduce this jitter is to speed up the rise/fall time of the input clock. Some chipsets may also require faster rise/fall time in order to reduce their sensitivity to this type of jitter. Refer to the Rise/Fall Time Tables (Table 7 to Table 11) to determine the proper drive strength.

### High Output Load Capability

The rise/fall time of the input clock varies as a function of the actual capacitive load the clock drives. At any given drive strength, the rise/fall time becomes slower as the output load increases. As an example, for a +3.3V MO2018 device with default drive strength setting, the typical rise/fall time is 1ns for 15 pF output load. The typical rise/fall time slows down to 2.6 ns when the output load increases to 45 pF. One can choose to speed up the rise/fall time to 1.83 ns by then increasing the drive strength setting on the MO2018.

The MO2018 can support up to 60 pF in maximum capacitive loads with drive strength settings. Refer to the Rise/Tall Time Tables (Table 7 to 11) to determine the proper drive strength for the desired combination of output load vs. rise/fall time

### MO2018 Drive Strength Selection

Tables 7 through 11 define the rise/fall time for a given capacitive load and supply voltage.

1. Select the table that matches the MO2018 nominal supply voltage (+1.8V, +2.5V, +2.8V, +3.0V, +3.3V).
2. Select the capacitive load column that matches the application requirement (5 pF to 60 pF)
3. Under the capacitive load column, select the desired rise/fall times.
4. The left-most column represents the part number code for the corresponding drive strength.
5. Add the drive strength code to the part number for ordering purposes.

### Calculating Maximum Frequency

Based on the rise and fall time data given in Tables 7 through 11, the maximum frequency the oscillator can operate with guaranteed full swing of the output voltage over temperature can be calculated as the following:

$$\text{Max Frequency} = \frac{1}{5 \times Trf\_20/80}$$

where Trf_20/80 is the typical value for 20%-80% rise/fall time.

***Example 1***

Calculate $f_{MAX}$ for the following condition:

- Vdd = +1.8V (Table 7)
- Capacitive Load: 30 pF
- Desired Tr/f time = 3 ns (rise/fall time part number code = E)

Part number for the above example:

MO2018EE5-C**E**H-18E0-0025000025

Drive strength code is here.

## Rise/Fall Time (20% to 80%) vs $C_{LOAD}$ Tables

### Table 7. Vdd = +1.8V Rise/Fall Times for Specific $C_{LOAD}$

| Rise/Fall Time Typ (ns) | | | | | |
|---|---|---|---|---|---|
| Drive Strength \ $C_{LOAD}$ | 5 pF | 15 pF | 30 pF | 45 pF | 60 pF |
| L | 6.16 | 11.61 | 22.00 | 31.27 | 39.91 |
| A | 3.19 | 6.35 | 11.00 | 16.01 | 21.52 |
| R | 2.11 | 4.31 | 7.65 | 10.77 | 14.47 |
| B | 1.65 | 3.23 | 5.79 | 8.18 | 11.08 |
| T | 0.93 | 1.91 | 3.32 | 4.66 | 6.48 |
| E | 0.78 | 1.66 | 2.94 | 4.09 | 5.74 |
| U | 0.70 | 1.48 | 2.64 | 3.68 | 5.09 |
| F or "0": default | 0.65 | 1.30 | 2.40 | 3.35 | 4.56 |

### Table 8. Vdd = +2.5V Rise/Fall Times for Specific $C_{LOAD}$

| Rise/Fall Time Typ (ns) | | | | | |
|---|---|---|---|---|---|
| Drive Strength \ $C_{LOAD}$ | 5 pF | 15 pF | 30 pF | 45 pF | 60 pF |
| L | 4.13 | 8.25 | 12.82 | 21.45 | 27.79 |
| A | 2.11 | 4.27 | 7.64 | 11.20 | 14.49 |
| R | 1.45 | 2.81 | 5.16 | 7.65 | 9.88 |
| B | 1.09 | 2.20 | 3.88 | 5.86 | 7.57 |
| T | 0.62 | 1.28 | 2.27 | 3.51 | 4.45 |
| E or "0": default | 0.54 | 1.00 | 2.01 | 3.10 | 4.01 |
| U | 0.43 | 0.96 | 1.81 | 2.79 | 3.65 |
| F | 0.34 | 0.88 | 1.64 | 2.54 | 3.32 |

### Table 9. Vdd = +2.8V Rise/Fall Times for Specific $C_{LOAD}$

| Rise/Fall Time Typ (ns) | | | | | |
|---|---|---|---|---|---|
| Drive Strength \ $C_{LOAD}$ | 5 pF | 15 pF | 30 pF | 45 pF | 60 pF |
| L | 3.77 | 7.54 | 12.28 | 19.57 | 25.27 |
| A | 1.94 | 3.90 | 7.03 | 10.24 | 13.34 |
| R | 1.29 | 2.57 | 4.72 | 7.01 | 9.06 |
| B | 0.97 | 2.00 | 3.54 | 5.43 | 6.93 |
| T | 0.55 | 1.12 | 2.08 | 3.22 | 4.08 |
| E or "0": default | 0.44 | 1.00 | 1.83 | 2.82 | 3.67 |
| U | 0.34 | 0.88 | 1.64 | 2.52 | 3.30 |
| F | 0.29 | 0.81 | 1.48 | 2.29 | 2.99 |

### Table 10. Vdd = +3.0V Rise/Fall Times for Specific $C_{LOAD}$

| Rise/Fall Time Typ (ns) | | | | | |
|---|---|---|---|---|---|
| Drive Strength \ $C_{LOAD}$ | 5 pF | 15 pF | 30 pF | 45 pF | 60 pF |
| L | 3.60 | 7.21 | 11.97 | 18.74 | 24.30 |
| A | 1.84 | 3.71 | 6.72 | 9.86 | 12.68 |
| R | 1.22 | 2.46 | 4.54 | 6.76 | 8.62 |
| B | 0.89 | 1.92 | 3.39 | 5.20 | 6.64 |
| T or "0": default | 0.51 | 1.00 | 1.97 | 3.07 | 3.90 |
| E | 0.38 | 0.92 | 1.72 | 2.71 | 3.51 |
| U | 0.30 | 0.83 | 1.55 | 2.40 | 3.13 |
| F | 0.27 | 0.76 | 1.39 | 2.16 | 2.85 |

### Table 11. Vdd = +3.3V Rise/Fall Times for Specific $C_{LOAD}$

| Rise/Fall Time Typ (ns) | | | | | |
|---|---|---|---|---|---|
| Drive Strength \ $C_{LOAD}$ | 5 pF | 15 pF | 30 pF | 45 pF | 60 pF |
| L | 3.39 | 6.88 | 11.63 | 17.56 | 23.59 |
| A | 1.74 | 3.50 | 6.38 | 8.98 | 12.19 |
| R | 1.16 | 2.33 | 4.29 | 6.04 | 8.34 |
| B | 0.81 | 1.82 | 3.22 | 4.52 | 6.33 |
| T or "0": default | 0.46 | 1.00 | 1.86 | 2.60 | 3.84 |
| E | 0.33 | 0.87 | 1.64 | 2.30 | 3.35 |
| U | 0.28 | 0.79 | 1.46 | 2.05 | 2.93 |
| F | 0.25 | 0.72 | 1.31 | 1.83 | 2.61 |

## Pin 3 Configuration Options (OE, $\overline{ST}$, or NC)

Pin 3 of the MO2018 can be factory-programmed to support three modes: Output Enable (OE), standby ($\overline{ST}$) or No Connect (NC).

### Output Enable (OE) Mode

In the OE mode, applying logic Low to the OE pin only disables the output driver and puts it in Hi-Z mode. The core of the device continues to operate normally. Power consumption is reduced due to the inactivity of the output. When the OE pin is pulled High, the output is typically enabled in <1µs.

### Standby ($\overline{ST}$) Mode

In the $\overline{ST}$ mode, a device enters into the standby mode when Pin 3 pulled Low. All internal circuits of the device are turned off. The current is reduced to a standby current, typically in the range of a few µA. When $\overline{ST}$ is pulled High, the device goes through the "resume" process, which can take up to 5 ms.

### No Connect (NC) Mode

In the NC mode, the device always operates in its normal mode and outputs the specified frequency regardless of the logic level on pin 3.

Table 12 below summarizes the key relevant parameters in the operation of the device in OE, $\overline{ST}$, or NC mode.

**Table 12. OE vs. $\overline{ST}$ vs. NC**

| | OE | $\overline{ST}$ | NC |
|---|---|---|---|
| Active current 20 MHz (max, +1.8V) | +4.5 mA | +4.5 mA | +4.5 mA |
| OE disable current (max. +1.8V) | +4.3 mA | N/A | N/A |
| Standby current (typical +1.8V) | N/A | +0.6 µA | N/A |
| OE enable time at 110 MHz (max) | 130 ns | N/A | N/A |
| Resume time from standby (max, all frequency) | N/A | 5.0 ms | N/A |
| Output driver in OE disable/standby mode | High Z | weak pull-down | N/A |

## Output on Startup and Resume

The MO2018 comes with gated output. Its clock output is accurate to the rated frequency stability within the first pulse from initial device startup or resume from the standby mode.

In addition, the MO2018 supports "no runt" pulses, and "no glitch" output during startup or resume as shown in the waveform captures in Figure 17 and Figure 18.

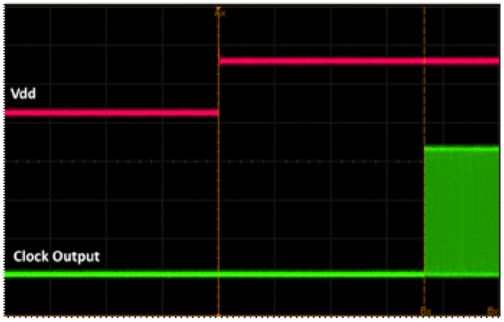



**Figure 17. Startup Waveform vs. Vdd**

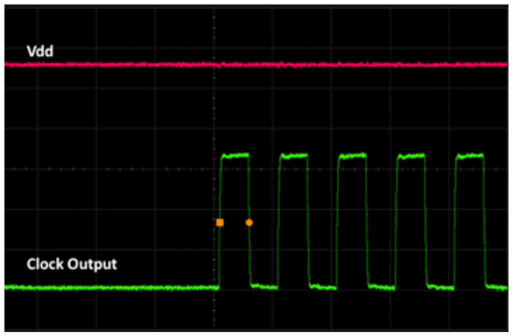
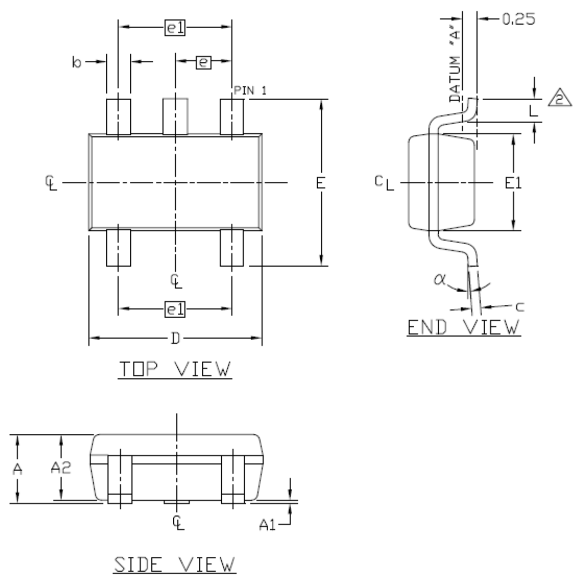



**Figure 18. Startup Waveform vs. Vdd (Zoomed-in View of Figure 17)**

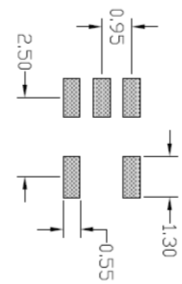
## Dimensions and Patterns

**Package Size – Dimensions (Unit: mm)[10]**

**2.90 x 2.80 mm SOT23-5**




**Recommended Land Pattern (Unit: mm)[11]**



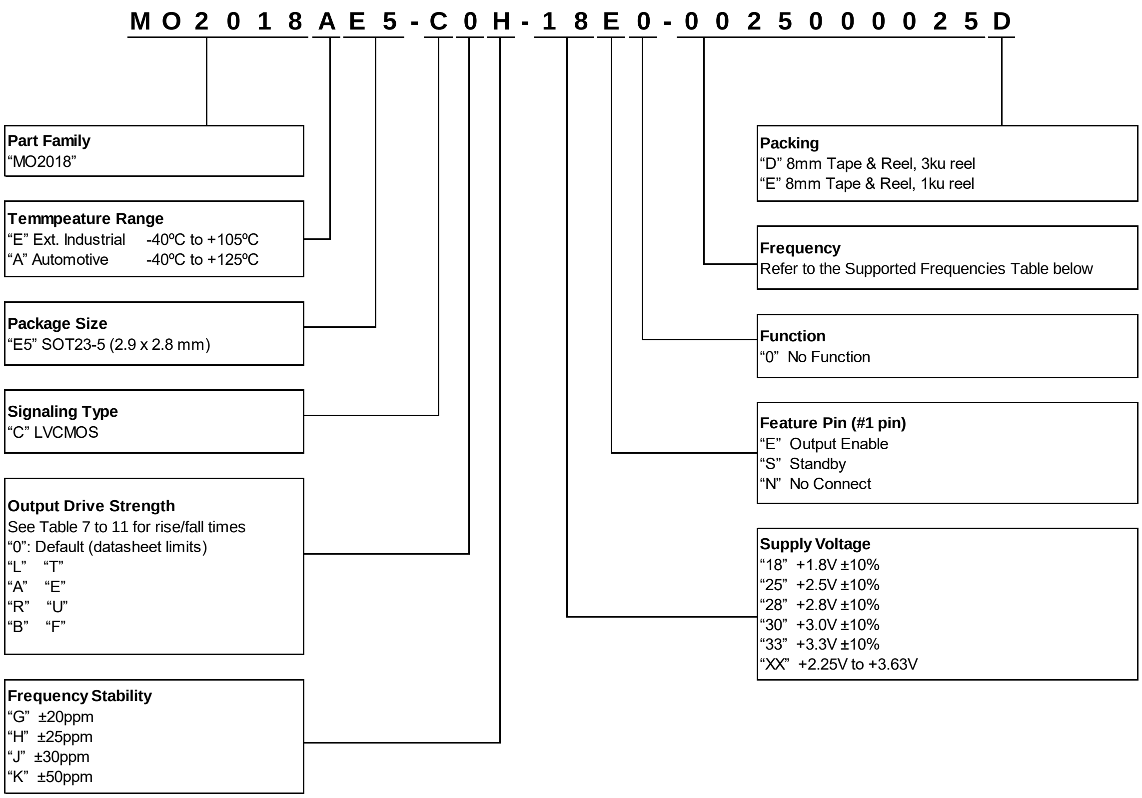

**Notes:**

10. Top marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
11. A capacitor value of 0.1 µF between Vdd and GND is required

### Table 13. Dimension Table

| Symbol | Min. | Nom. | Max. |
|---|---|---|---|
| A | 0.90 | 1.27 | 1.45 |
| A1 | 0.00 | 0.07 | 0.15 |
| A2 | 0.90 | 1.20 | 1.30 |
| b | 0.30 | 0.35 | 0.50 |
| c | 0.14 | 0.15 | 0.20 |
| D | 2.75 | 2.90 | 3.05 |
| E | 2.60 | 2.80 | 3.00 |
| E1 | 1.45 | 1.60 | 1.75 |
| L | 0.30 | 0.38 | 0.55 |
| L1 | 0.25 REF | | |
| e | 0.95 BSC. | | |
| e1 | 1.90 BSC. | | |
| α | 0° | – | 8° |

## Ordering Information




## Table 14. List of Supported Frequencies[12, 13]

| Frequency Range (-40 to +105°C or -40 to +125°C) | |
|---|---|
| **Min.** | **Max.** |
| 1.000000 MHz | 61.222999 MHz |
| 61.674001 MHz | 69.795999 MHz |
| 70.485001 MHz | 79.062999 MHz |
| 79.162001 MHz | 81.427999 MHz |
| 82.232001 MHz | 91.833999 MHz |
| 92.155001 MHz | 94.248999 MHz |
| 94.430001 MHz | 94.874999 MHz |
| 94.994001 MHz | 97.713999 MHz |
| 98.679001 MHz | 110.000000 MHz |

**Notes:**

12. Any frequency within the min and max values in the above table are supported with 6 decimal places of accuracy.
13. Please contact KDS for frequencies that are not listed in the tables above.

## Revision History

### Table 15. Datasheet Version and Change Log

| Version | Release Date | Change Summary |
|---|---|---|
| 1.0 | 05/14/2015 | Final Production Release. |
| 1.01 | 09/29/2015 | • Revised the dimension table |
| 1.02 | 04/27/2015 | • Changed Clock Generator to SOT23 Oscillator |