

#### **Features**

- Any frequency between 1 MHz and 220 MHz accurate to 6 decimal places
- Widest pull range options: ±25, ±50, ±80, ±100, ±150, ±200, ±400, ±800, ±1600, ±3200 ppm
- 0.23ps RMS phase jitter (Typ) over 12 kHz to 20 MHz bandwidth
- Wide temperature range from -40°C to +105°C
- Industry-standard packages: 3.2x2.5, 5.0x3.2, 7.0x5.0 mm
- For frequencies 220.000001 MHz to 720 MHz, refer to MO3373 datasheet

## **Applications**

- Cable Modern Termination System (CMTS), Video, Broadcasting System, Audio, Industrial Sensors, Remote Radio Head (RRH)
- SATA, SAS, 10GB Ethernet, Fibre Channel, PCI-Express





### **Electrical Characteristics**

#### Table 1. Electrical Characteristics - Common to LVPECL, LVDS and HCSL

All Min and Max limits in the Electrical Characteristics tables are specified over temperature and rated operating voltage with standard output termination show in the termination diagrams. Typical values are at +25°C and nominal supply voltage.

Parameter	Symbol	Min.	Тур.	Max.	Unit	Condition
			F	requency Ra	ange	
Output Frequency Range	f	1	-	220	MHz	Accurate to 6 decimal places
		•	Fr	equency Sta	bility	
		-15	-	+15	ppm	
5	C -4-b	-20	-	+20	ppm	Inclusive of initial tolerance, operating temperature, rated power
Frequency Stability	F_stab	-30	-	+30	ppm	supply voltage, load variations, and first year aging at +25°C. Contact KDS for ±15 ppm.
		-50	-	+50	ppm	1
			Те	mperature R	lange	
		-20	-	+70	°C	Extended Commercial
One retire Temperature Banco	T use	-40	-	+85	°C	Industrial.
Operating Temperature Range	1_use	-40	-	+95	°C	
		-40	-	+105	°C	Extended Industrial
				Supply Volta	age	
		+2.97	+3.3	+3.63	V	
	Vdd	+2.7	+3.0	+3.3	V	
Supply Voltage		+2.52	+2.8	+3.08	V	
		+2.25	+2.5	+2.75	V	
			Voltage	Control Cha	racteristics	5
Pull Range	PR	±25, ±50, ±80, ±100, ±150, ±200,				See the APR (Absolute Pull Range) Table 11.
Full Kange	PK	±400, :	±800, ±1600	, ±3200	ppm	Contact KDS for custom pull range options.
Upper Control Voltage	VC_U	90%	_	-	Vdd	Voltage at which maximum frequency deviation is guaranteed
Lower Control Voltage	VC_L	-	-	10%	Vdd	Voltage at which minimum frequency deviation is guaranteed
Control Voltage Input Impedance	VC_z	-	10	_	ΜΩ	
Control Voltage Input Bandwidth	V_c	-	10	_	kHz	Contact KDS for other input bandwidth options
Pull Range Linearity	Lin	-	-	1.0	%	
Frequency Change Polarity	-	F	Positive Slop		-	
		1	Inp	ut Characte		т
Input Voltage High	VIH	70%	-	-	Vdd	Pin 2, OE
Input Voltage Low	VIL	-	-	30%	Vdd	Pin 2, OE
Input Pull-up Impedance	Z_in	-	100	-	kΩ	Pin 2, OE logic high or logic low
		ı	Out	put Charact	eristics	1
Duty Cycle	DC	45	-	55	%	
			Sta	rtup and OE	Timing	
Start-up Time	T_start	-	-	3.0	ms	Measured from the time Vdd reaches its rated minimum value.
OE Enable/Disable Time	T_oe	_	-	3.8	μs	f = 156.25 MHz. Measured from the time OE pin reaches rated VIH and VIL to the time clock pins reach 90% of swing and high-Z. See Figure 7 and Figure 8.

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## **Table 2. Electrical Characteristics - LVPECL Specific**

Parameter	Symbol	Min.	Тур.	Max.	Unit	Condition	
			C	urrent Co	nsumpti	on	
Current Consumption	ldd	_	-	+92	mA	Excluding Load Termination Current, Vdd = +3.3V or +2.5V	
OE Disable Supply Current	I_OE	-	-	+61	mA	OE = Low	
Output Disable Leakage Current	l_leak	-	+0.15	-	μА	OE = Low	
Maximum Output Current	I_driver	-	-	+33	mA	Maximum average current drawn from OUT+ or OUT-	
			C	output Cha	racteris	tics	
Output High Voltage	VOH	Vdd-1.15	ı	Vdd-0.7	V	See Figure 3	
Output Low Voltage	VOL	Vdd-2.0	ı	Vdd-1.5	V	See Figure 3	
Output Differential Voltage Swing	V_Swing	+1.2	+1.6	+2.0	V	See Figure 3	
Rise/Fall Time	Tr, Tf	_	225	290	ps	20% to 80%, See Figure 4	
	Jitter – 7.0 x 5.0 mm package						
RMS Period Jitter[1]	T_jitt	-	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, VDD = +3.3V or +2.5V	
		-	0.225	0.270	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels. Includes spurs, pull range = 100 ppm. Temperature range -20 to +70°C and -40 to +85°C.	
RMS Phase Jitter (random)	T_phj	-	0.225	0.300	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels. Includes spurs, pull range = 100 ppm. Temperature range -40 to +95°C and -40 to +105°C.	
		-	0.1	-	ps	f = 156.25, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all Vdd levels.	
		Jtter	– 5.0 x 3	3.2 mm an	d 3.2 x 2	.5 mm package	
RMS Period Jitter <sup>[1]</sup>	T_jitt	_	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, VDD = +3.3V or +2.5V	
	T_phj	-	0.225	0.275	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels. Includes spurs, pull range = 100 ppm. Temperature range -20 to +70°C and -40 to +85°C.	
RMS Phase Jitter (random)		-	0.225	0.340	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels. Includes spurs, pull range = 100 ppm. Temperature range -40 to +95°C and -40 to +105°C.	
		-	0.1	-	ps	f = 156.25 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all Vdd levels.	

#### Notes:

1. Measured according to JESD65B.

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Table 3. Electrical Characteristics – LVDS Specific

Parameter	Symbol	Min.	Тур.	Max.	Unit	Condition		
			Cı	rrent Co	nsump	otion		
Current Consumption	ldd	-	_	+84	mA	Excluding Load Termination Current, Vdd = +3.3V or +2.5V		
OE Disable Supply Current	I_OE	-	_	+62	mA	OE = Low		
Output Disable Leakage Current	l_leak	-	+0.15	ı	μΑ	OE = Low		
	Output Characteristics							
Differential Output Voltage	VOD	+250	_	+450	mV	See Figure 5		
VOD Magnitude Change	ΔVOD	-	_	+50	mV	See Figure 5		
Offset Voltage	VOS	+1.125	_	+1.375	V	See Figure 5		
VOS Magnitude Change	ΔVOS	-	_	+50	mV	See Figure 5		
Rise/Fall Time	Tr, Tf	_	400	470	ps	Measured with 2 pF capacitive loading to GND, 20% to 80%, see Figure 6		
Jitter – 7.0 x 5.0 mm package								
RMS Period Jitter[2]	T_jitt	-	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, VDD = +3.3V or +2.5V		
		-	0.215	0.265	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels. Includes spurs, pull range = 100 ppm. Temperature range -20 to +70°C and -40 to +85°C.		
RMS Phase Jitter (random)	T_phj	-	0.215	0.300	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels. Includes spurs, pull range = 100 ppm. Temperature range -40 to +95°C and -40 to +105°C.		
		-	0.1	-	ps	f = 156.25 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all Vdd levels.		
		Jtter	– 5.0 x 3	.2 mm an	d 3.2 x 2	.5 mm package		
RMS Period Jitter <sup>[2]</sup>	T_jitt	_	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, VDD = +3.3V or +2.5V		
		-	0.235	0.275	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels. Includes spurs, pull range = 100 ppm. Temperature range -20 to +70°C and -40 to +85°C.		
RMS Phase Jitter (random)	T_phj	-	0.235	0.320	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels. Includes spurs, pull range = 100 ppm. Temperature range -40 to +95°C and -40 to +105°C.		
		-	0.1	-	ps	f = 156.25 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all Vdd levels.		

#### Notes:

2. Measured according to JESD65B.

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Table 4. Electrical Characteristics – HCSL Specific

Parameter	Symbol	Min.	Тур.	Max.	Unit	Condition		
Current Consumption								
Current Consumption	ldd	_	_	+97	mA	Excluding Load Termination Current, Vdd = +3.3V or +2.5V		
OE Disable Supply Current	I_OE	_	_	+62	mA	OE = Low		
Output Disable Leakage Current	l_leak	-	+0.15	-	μА	OE = Low		
Maximum Output Current	l_driver	-	-	+35	mA	Maximum average current drawn from OUT+ or OUT-		
			Ot	itput Cha	racterist	tics		
Output High Voltage	VOH	+0.60	_	+0.90	V	See Figure 3		
Output Low Voltage	VOL	-0.05	_	+0.08	V	See Figure 3		
Output Differential Voltage Swing	V_Swing	+1.2	+1.4	+1.8	V	See Figure 4		
Rise/Fall Time	Tr, Tf	ı	360	495	ps	Measured with 2 pF capacitive loading to GND, 20% to 80%, see Figure 4		
Jitter – 7.0 x 5.0 mm package								
RMS Period Jitter <sup>[3]</sup>	T_jitt	_	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, VDD = +3.3V or +2.5V		
		-	0.220	0.270	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels. Includes spurs, pull range = 100 ppm. Temperature range -20 to +70°C and -40 to +85°C.		
RMS Phase Jitter (random)	T_phj	-	0.220	0.300	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels. Includes spurs, pull range = 100 ppm. Temperature range -40 to +95°C and -40 to +105°C.		
		-	0.1	-	ps	f = 156.25 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all Vdd levels.		
		Jtter	- 5.0 x 3	.2 mm an	d 3.2 x 2	.5 mm package		
RMS Period Jitter[3]	T_jitt	-	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, VDD = +3.3V or +2.5V		
		1	0.230	0.275	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels. Includes spurs, pull range = 100 ppm. Temperature range -20 to +70°C and -40 to +85°C.		
RMS Phase Jitter (random)	T_phj	ı	0.230	0.340	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels. Includes spurs, pull range = 100 ppm. Temperature range -40 to +95°C and -40 to +105°C.		
		-	0.1	-	ps	f = 156.25 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all Vdd levels.		

#### Notes:

3. Measured according to JESD65B.



## **Table 5. Pin Description**

Pin	Мар	Functionality				
1	VIN	Input	Control Voltage			
		Non Connect (NC)	No Connect: Leave it floating or connect to GND for better heat dissipation. NC for all 3.2 x 2.5 mm package options.			
2	OE/NC	Output Enable (OE)	H <sup>[4,5]</sup> : specified frequency output L: output is high impedance. Only output driver is disabled. OE function only available on 7050 and 5032 package. Pin 2 on 3225 package is NC.			
3	GND	Power	VDD Power Supply Ground			
4	OUT+	Output Oscillator output				
5	OUT-	Output	Complementary oscillator output			
6	VDD	Power	Power supply voltage <sup>[6]</sup>			

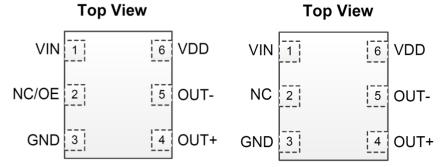


Figure 1. Pin Assignments (7.0 x 5.0 mm and 5.0 x 3.2 mm packgages)

Figure 2. Pin Assignments (3.2 x 2.5 mm package)

#### Notes:

- 4. A pull-up resistor of 10  $k\Omega$  or less is recommended if pin 1 is not externally driven.
- 5. OE mode is only available in the 7050 and 5032 package. 3225 package is NC.
- 6. A capacitor of value 0.1 μF or higher between Vdd and GND is required. An additional 10 μF capacitor between Vdd and GND is required for the best phase jitter performance.

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## **Table 6. Absolute Maximum Ratings**

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
VDD	-0.5	+4.0	V
VIH	-	Vdd + 0.3	V
VIL	-0.3	-	V
Storage Temperature	-65	+150	°C
Maximum Junction Temperature	-	+130	°C
Soldering Temperature (follow standard Pb free soldering guidelines)	_	+260	°C

#### Table 7. Thermal Consideration<sup>[7]</sup>

Package	θJA, 4 Layer Board (°C/W)	θJC, Bottom (°C/W)
3225, 6-pin	80	30
5032, 6-pin	TBD	TBD
7050, 6-pin	52	19

#### Notes:

## Table 8. Maximum Operating Junction Temperature<sup>[8]</sup>

Max Operating Temperature (ambient)	Maximum Operating Junction Temperature
+70°C	+95°C
+85°C	+110°C
+95°C	+120°C
+105°C	+130°C

#### Notes:

## **Table 9. Environmental Compliance**

Parameter	Test Conditions	Value	Unit
Mechanical Shock Resistance	MIL-STD-883F, Method 2002	10,000	g
Mechanical Vibration Resistance	MIL-STD-883F, Method 2007	70	g
Soldering Temperature (follow standard Pb free soldering guidelines)	MIL-STD-883F, Method 2003	260	°C
Moisture Sensitivity Level	MSL1 @ +260°C		
Electrostatic Discharge (HBM)	HBM, JESD22-A114	20,000	V
Charge-Device Model ESD Protection	JESD220C101	750	V
Latch-up Tolerance	JESD78 (	Compliant	

<sup>7.</sup> Refer to JESD51 for  $\theta_{JA}$  and  $\theta_{JC}$  definitions, and reference layout used to determine the  $\theta_{JA}$  and  $\theta_{JC}$  values in the above table.

<sup>8.</sup> Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.



# **Waveform Diagrams**

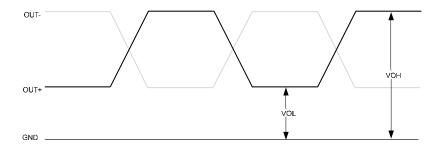


Figure 3. LVPECL/HCSL Voltage Levels per Differential Pin (OUT+/OUT-)

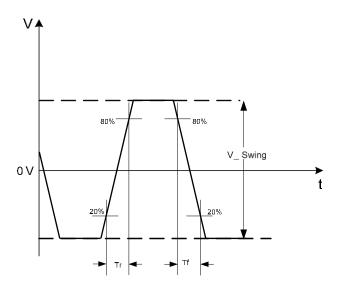


Figure 4. LVPECL/HCSL Voltage Levels across Differential Pair



# **Waveform Diagrams(continued)**

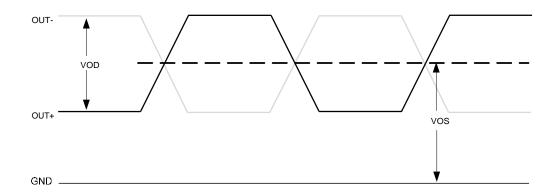


Figure 5. LVDS Voltage Levels per Differential Pin (OUT+/OUT-)

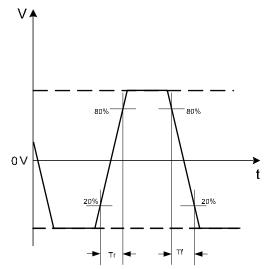


Figure 6. LVDS Differential Waveform

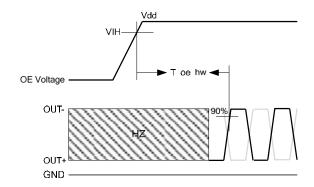


Figure 7. Hardware OE Enable Timing

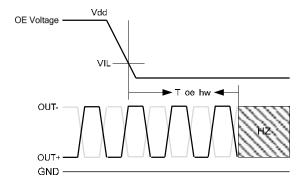


Figure 8. Hardware OE Disable Timing



## **Termination Diagrams**

## LVPECL:

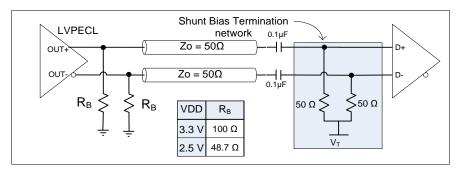


Figure 9. LVPECL with AC-coupled termination

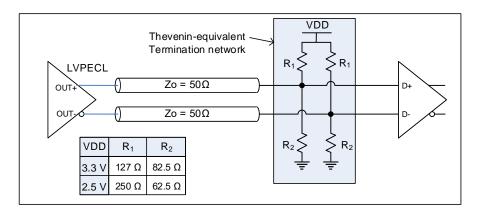


Figure 10. LVPECL DC-coupled load termination with Thevenin equivalent network

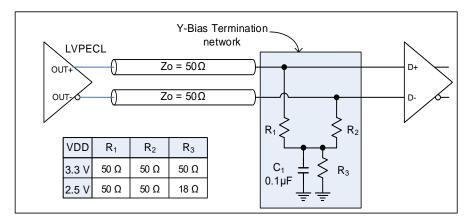


Figure 11. LVPECL with Y-Bias termination



# **Termination Diagrams (Continued)**

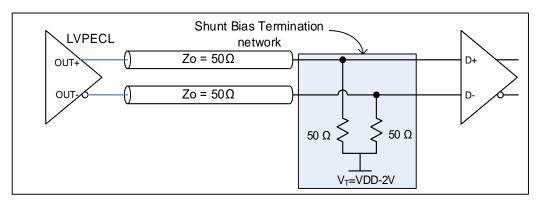


Figure 12. LVPECL with DC-coupled parallel shunt load termination



## **Termination Diagrams (Continued)**

LVDS:

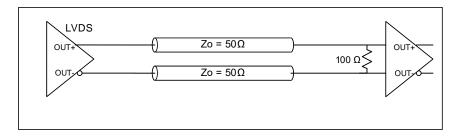


Figure 13. LVDS single DC termination at the load

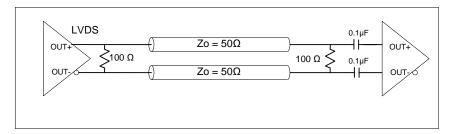


Figure 14. LVDS double AC termination with capacitor close to the load

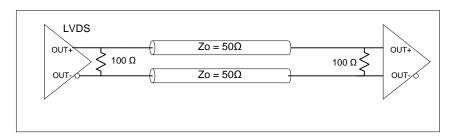


Figure 15. LVDS double DC termination

**HCSL**:

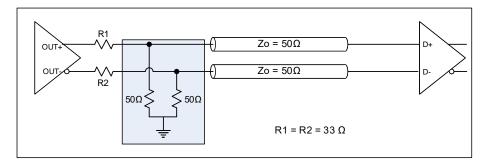
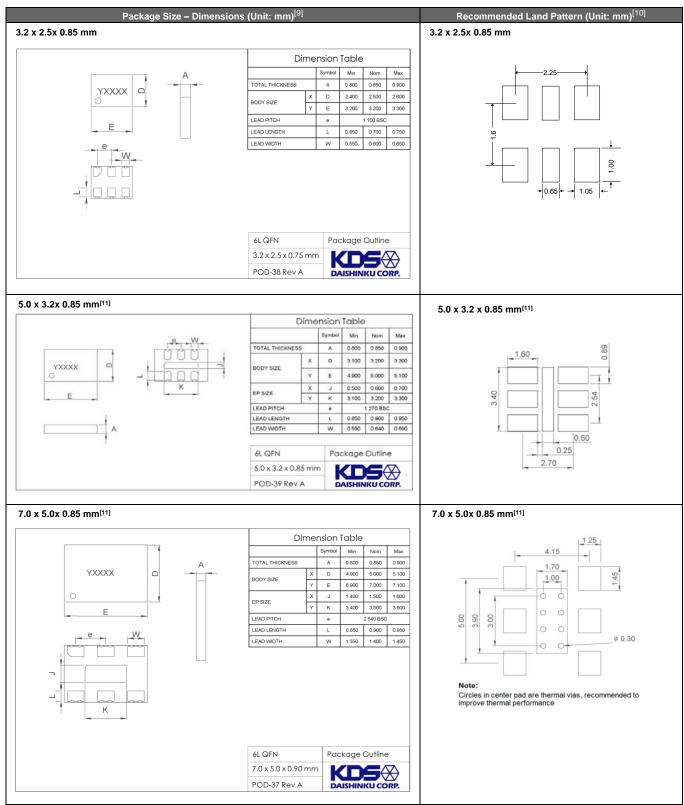


Figure 16. HCSL interface termination



#### **Dimensions and Patterns**

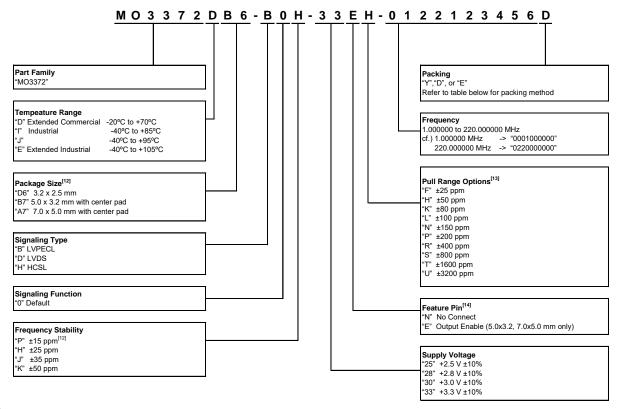


#### Notes:

- 9. Top Marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
- 10. A capacitor of value 0.1 μF or higher between Vdd and GND is required. An additional 10 μF capacitor between Vdd and GND is required for the best phase litter performance
- 11. The center pad has no electrical function. Soldering down the center pad to the GND is recommended for best thermal dissipation, but is optional.



## **Ordering Information**



#### Notes:

- 12. Contact KDS for ±15 ppm
- 13. Contact KDS for custom pull range options
- 14. "E": Output Enable function is only available in 7.0 x 5.0 mm and 5.0 x 3.2 mm packages

Table 10. Ordering Codes for Supported Tape & Reel Packing Method

Device Size (mm x mm)	8 mm T&R (3ku)	8 mm T&R (1ku)	12 mm T&R (3ku)	12 mm T&R (1ku)	16 mm T&R (3ku)	16 mm T&R (1ku)
7.0 x 5.0 mm	-	-	-	-	-	Y
5.0 x 3.2 mm	-	-	-	Υ	-	-
3.2 x 2.5 mm	D	Е	-	-	-	-

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## Table 11. APR Table

Absolute pull range (APR) = Nominal pull range (PR) - frequency stability (F\_stab)-aging

		Frequency Stability					
Nominal Pull Range	± 15	± 25	± 35	± 50			
		APR	(ppm)				
± 25	± 5	_	-	_			
± 50	± 30	± 20	± 10	_			
± 80	± 60	± 50	± 40	± 25			
± 100	± 80	± 70	± 60	± 45			
± 150	± 130	± 120	± 110	± 95			
± 200	± 180	± 170	± 160	± 145			
± 400	± 380	± 370	± 360	± 345			
± 800	± 780	± 770	± 760	± 745			
± 1600	± 1580	± 1570	± 1560	± 1545			
± 3200	± 3180	± 3170	± 3160	± 3145			

# **Table 12. Revision History**

Revision	Release Date	Change Summary
1.0	10/13/2017	Initial release
1.03	05/10/2018	Updated the Part Ordering info with added 5.0 x 3.2 mm package