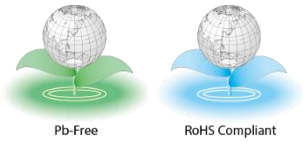
MO3373
220 to 725 MHz Ultra-low Jitter Differential VCMO

Features

- Any frequency between 220.000001 MHz and 725 MHz accurate to 6 decimal places
- Widest pull range options: ±25, ±50, ±80, ±100, ±150, ±200, ±400, ±800, ±1600, ±3200 ppm
- 0.23ps RMS phase jitter (Typ.) over 12 kHz to 20 MHz bandwidth
- Wide temperature range from -40°C to +105°C
  Contact KDS for higher temperature range options
- Industry-standard packages: 3.2x2.5, 5.0x3.2, 7.0x5.0 mm
- For frequencies 10 MHz to 220 MHz, refer to MO3372

Applications

- Remote Radio Head (RRH), Cable Modem Termination System (CMTS), Video, Broadcasting System, Audio, Industrial Sensors
- SATA, SAS, 10GB Ethernet, Fibre Channel, PCI-Express
- Optical Transport Network (OTN)



Electrical Characteristics

Table 1. Electrical Characteristics - Common to LVPECL, LVDS and HCSL

All Min and Max limits in the Electrical Characteristics tables are specified over temperature and rated operating voltage with standard output termination show in the termination diagrams. Typical values are at +25°C and nominal supply voltage.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Range						
Output Frequency Range	f	220.000001	–	725	MHz	Accurate to 6 decimal places
Frequency Stability						
Frequency Stability	F_stab	-15	–	+15	ppm	Inclusive of initial tolerance, operating temperature, rated power supply voltage, load variations, and first year aging at +25°C. Contact KDS for ±15 ppm.
		-25	–	+25	ppm	
		-30	–	+30	ppm	
		-50	–	+50	ppm	
Temperature Range						
Operating Temperature Range	T_use	-20	–	+70	°C	Extended Commercial
		-40	–	+85	°C	Industrial.
		-40	–	+95	°C	
		-40	–	+105	°C	Extended Industrial.
Supply Voltage						
Supply Voltage	Vdd	+2.97	+3.3	+3.63	V	
		+2.7	+3.0	+3.3	V	
		+2.52	+2.8	+3.08	V	
		+2.25	+2.5	+2.75	V	
Voltage Control Characteristics						
Pull Range	PR	±25, ±50, ±80, ±100, ±150, ±200, ±400, ±800, ±1600, ±3200			ppm	See the Absolute Pull Range, APR Table 11. Contact KDS for custom pull range options.
Upper Control Voltage	VC_U	90%	–	–	Vdd	Voltage at which maximum frequency deviation is guaranteed
Lower Control Voltage	VC_L	–	–	10%	Vdd	Voltage at which minimum frequency deviation is guaranteed
Control Voltage Input Impedance	VC_z	–	10	–	MΩ	
Control Voltage Input Bandwidth	V_c	–	10	–	kHz	Contact KDS for other input bandwidth options
Pull Range Linearity	Lin	–	–	1.0	%	
Frequency Change Polarity	–	Positive Slope			–	
Input Characteristics						
Input Voltage High	VIH	70%	–	–	Vdd	Pin 2, OE
Input Voltage Low	VIL	–	–	30%	Vdd	Pin 2, OE
Input Pull-up Impedance	Z_in	–	100	-	kΩ	Pin 2, OE logic high or logic low
Output Characteristics						
Duty Cycle	DC	45	–	55	%	
Startup and OE Timing						
Start-up Time	T_start	–	–	3.0	ms	Measured from the time Vdd reaches its rated minimum value.
OE Enable/Disable Time	T_oe	–	–	3.8	µs	f = 322.265625 MHz. Measured from the time OE pin reaches rated VIH and VIL to the time clock pins reach 90% of swing and high-Z. See Figure 7 and Figure 8.

Table 2. Electrical Characteristics - LVPECL Specific

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption	Idd	–	–	+97	mA	Excluding Load Termination Current, Vdd = +3.3V or +2.5V
OE Disable Supply Current	I_OE	–	–	+63	mA	OE = Low
Output Disable Leakage Current	I_leak	–	+0.15	–	µA	OE = Low
Maximum Output Current	I_driver	–	–	+32	mA	Maximum average current drawn from OUT+ or OUT-
Output Characteristics						
Output High Voltage	VOH	Vdd-1.15	–	Vdd-0.7	V	See Figure 3
Output Low Voltage	VOL	Vdd-1.9	–	Vdd-1.5	V	See Figure 3
Output Differential Voltage Swing	V_Swing	+1.2	+1.6	+2.0	V	See Figure 4
Rise/Fall Time	Tr, Tf	–	225	290	ps	20% to 80%, See Figure 4
Jitter – 7.0 x 5.0 mm package						
RMS Period Jitter[1]	T_jitt	–	1.0	1.6	ps	f = 322.265625 MHz, VDD = +3.3V or +2.5V Pull Range = 100 ppm.
RMS Phase Jitter (random)	T_phj	–	0.220	0.270	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels. Includes spurs, pull range = 100 ppm. Temperature range -20 to +70°C and -40 to +85°C.
		–	0.220	0.300	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels. Includes spurs, pull range = 100 ppm. Temperature range -40 to +95°C and -40 to +105°C.
		–	0.1	–	ps	f = 322.265625MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all Vdd levels.
Jitter – 5.0 x 3.2 mm and 3.2 x 2.5 mm package						
RMS Period Jitter[1]	T_jitt	–	1.0	1.6	ps	f = 322.265625 MHz, VDD = +3.3V or +2.5V Pull Range = 100 ppm.
RMS Phase Jitter (random)	T_phj	–	0.225	0.282	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels. Includes spurs, pull range = 100 ppm. Temperature range -20 to +70°C and -40 to +85°C.
		–	0.225	0.315	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels. Includes spurs, pull range = 100 ppm. Temperature range -40 to +95°C and -40 to +105°C.
		–	0.1	–	ps	f = 322.265625MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all Vdd levels.

Notes:

1. Measured according to JESD65B.

Table 3. Electrical Characteristics – LVDS Specific

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption	Idd	–	–	+89	mA	Excluding Load Termination Current, Vdd = +3.3V or +2.5V
OE Disable Supply Current	I_OE	–	–	+67	mA	OE = Low
Output Disable Leakage Current	I_leak	–	+0.15	–	µA	OE = Low
Output Characteristics						
Differential Output Voltage	VOD	+250	–	+450	mV	See Figure 5
VOD Magnitude Change	ΔVOD	–	–	+50	mV	See Figure 5
Offset Voltage	VOS	+1.125	–	+1.375	V	See Figure 5
VOS Magnitude Change	ΔVOS	–	–	+50	mV	See Figure 5
Rise/Fall Time	Tr, Tf	–	370	470	ps	Measured with 2 pF capacitive loading to GND, 20% to 80%, see Figure 6
Jitter – 7.0 x 5.0 mm package						
RMS Period Jitter[2]	T_jitt	–	0.92	1.6	ps	f = 322.265625 MHz, VDD = +3.3V or +2.5V Pull Range = 100 ppm.
RMS Phase Jitter (random)	T_phj	–	0.215	0.265	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels. Includes spurs, pull range = 100 ppm. Temperature range -20 to +70°C and -40 to +85°C.
		–	0.215	0.280	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels. Includes spurs, pull range = 100 ppm. Temperature range -40 to +95°C and -40 to +105°C.
		–	0.1	–	ps	f = 322.265625MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all Vdd levels.
Jitter – 5.0 x 3.2 mm and 3.2 x 2.5 mm package						
RMS Period Jitter[2]	T_jitt	–	0.92	1.6	ps	f = 322.265625 MHz, VDD = +3.3V or +2.5V Pull Range = 100 ppm.
RMS Phase Jitter (random)	T_phj	–	0.235	0.282	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels. Includes spurs, pull range = 100 ppm. Temperature range -20 to +70°C and -40 to +85°C.
		–	0.235	0.310	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels. Includes spurs, pull range = 100 ppm. Temperature range -40 to +95°C and -40 to +105°C.
		–	0.1	–	ps	f = 322.265625MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all Vdd levels.

Notes:

2. Measured according to JESD65B.

Table 4. Electrical Characteristics – HCSL Specific

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption	Idd	–	–	+102	mA	Excluding Load Termination Current, Vdd = +3.3V or +2.5V
OE Disable Supply Current	I_OE	–	–	+67	mA	OE = Low
Output Disable Leakage Current	I_leak	–	+0.15	–	µA	OE = Low
Maximum Output Current	I_driver	–	–	+36	mA	Maximum average current drawn from OUT+ or OUT-
Output Characteristics						
Output High Voltage	VOH	+0.60	–	+0.90	V	See Figure 3
Output Low Voltage	VOL	-0.05	–	+0.08	V	See Figure 3
Output Differential Voltage Swing	V_Swing	+1.2	+1.4	+1.8	V	See Figure 4
Rise/Fall Time	Tr, Tf	–	360	470	ps	Measured with 2 pF capacitive loading to GND, 20% to 80%, see Figure 4
Jitter – 7.0 x 5.0 mm package						
RMS Period Jitter[3]	T_jitt	–	1.0	1.6	ps	f = 322.265625 MHz, VDD = +3.3V or +2.5V
RMS Phase Jitter (random)	T_phj	–	0.215	0.265	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels. Includes spurs, pull range = 100 ppm. Temperature range -20 to +70°C and -40 to +85°C.
		–	0.215	0.282	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels. Includes spurs, pull range = 100 ppm. Temperature range -40 to +95°C and -40 to +105°C.
		–	0.1	–	ps	f = 322.265625MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all Vdd levels.
Jitter – 5.0 x 3.2 mm and 3.2 x 2.5 mm package						
RMS Period Jitter[3]	T_jitt	–	1.0	1.6	ps	f = 322.265625 MHz, VDD = +3.3V or +2.5V
RMS Phase Jitter (random)	T_phj	–	0.235	0.282	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels. Includes spurs, pull range = 100 ppm. Temperature range -20 to +70°C and -40 to +85°C.
		–	0.235	0.305	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels. Includes spurs, pull range = 100 ppm. Temperature range -40 to +95°C and -40 to +105°C.
		–	0.1	–	ps	f = 322.265625MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all Vdd levels.

Notes:

3. Measured according to JESD65B.

Table 5. Pin Description

Pin	Map	Functionality	
1	VIN	Input	Control Voltage
2	OE/NC	Non Connect (NC)	No Connect: Leave it floating or connect to GND for better heat dissipation. NC for all 3.2 x 2.5 mm package options.
		Output Enable (OE)	H[4,5]: specified frequency output L: output is high impedance. Only output driver is disabled. OE function only available on 7050 and 5032 package. Pin 2 on 3225 package is NC.
3	GND	Power	Vdd Power Supply Ground
4	OUT+	Output	Oscillator output
5	OUT-	Output	Complementary oscillator output
6	VDD	Power	Power supply voltage[6]

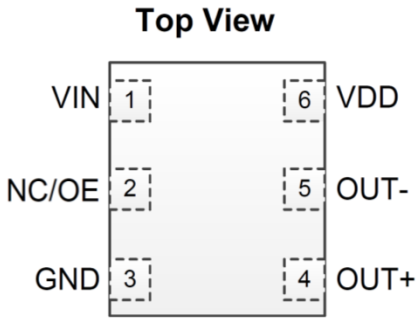


Figure 1. Pin Assignments (7.0 x 5.0 mm and 5.0 x 3.2 mm packgages)

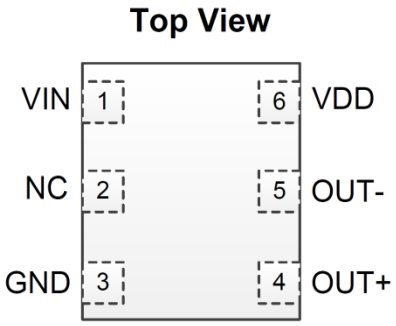


Figure 2. Pin Assignments (3.2 x 2.5 mm package)

Notes:

4. A pull-up resistor of 10 kΩ or less is recommended if pin 1 is not externally driven.
5. OE mode is only available in the 7050 and 5032 package. 3225 package is NC.
6. A capacitor of value 0.1 µF or higher between Vdd and GND is required. An additional 10 µF capacitor between Vdd and GND is required for the best phase jitter performance.

Table 6. Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
VDD	-0.5	+4.0	V
VIH	–	Vdd + 0.3	V
VIL	-0.3	–	V
Storage Temperature	-65	+150	°C
Maximum Junction Temperature	–	+130	°C
Soldering Temperature (follow standard Pb free soldering guidelines)	–	+260	°C

Table 7. Thermal Considerations[7]

Package	θJA, 4 Layer Board (°C/W)	θJC, Bottom (°C/W)
3225, 6-pin	80	30
5032, 6-pin	TBD	TBD
7050, 6-pin	52	19

Notes:

7. Refer to JESD51 for θ_{JA} and θ_{JC} definitions, and reference layout used to determine the θ_{JA} and θ_{JC} values in the above table.

Table 8. Maximum Operating Junction Temperature[8]

Max Operating Temperature (ambient)	Maximum Operating Junction Temperature
+70°C	+95°C
+85°C	+110°C
+95°C	+120°C
+105°C	+130°C

Notes:

8. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

Table 9. Environmental Compliance

Parameter	Test Conditions	Value	Unit
Mechanical Shock Resistance	MIL-STD-883F, Method 2002	10,000	g
Mechanical Vibration Resistance	MIL-STD-883F, Method 2007	70	g
Soldering Temperature (follow standard Pb free soldering guidelines)	MIL-STD-883F, Method 2003	260	°C
Moisture Sensitivity Level	MSL1 @ +260°C		
Electrostatic Discharge (HBM)	HBM, JESD22-A114	20,000	V
Charge-Device Model ESD Protection	JESD220C101	750	V
Latch-up Tolerance	JESD78 Compliant		

Waveform Diagrams

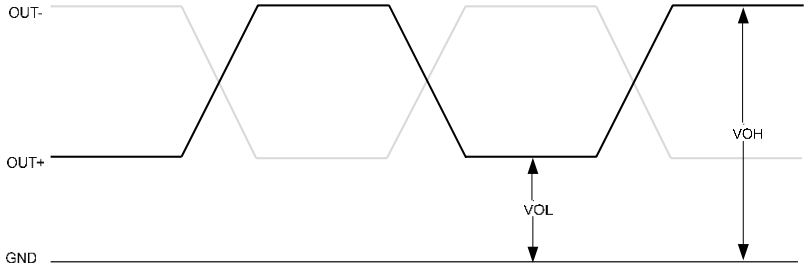


Figure 3. LVPECL/HCSL Voltage Levels per Differential Pin (OUT+/OUT-)

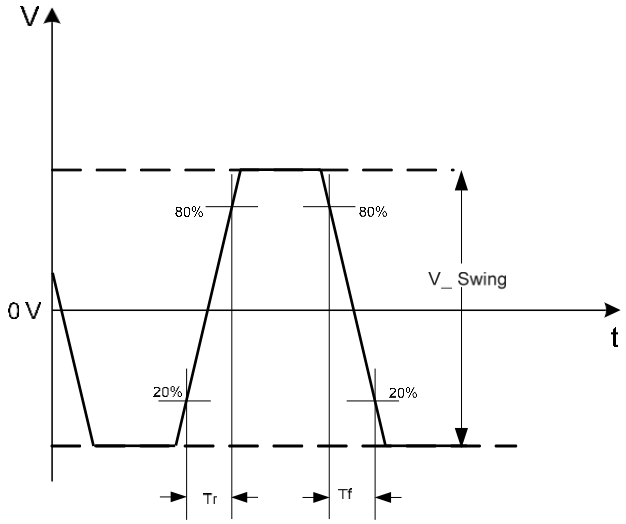


Figure 4. LVPECL/HCSL Voltage Levels across Differential Pair

Waveform Diagrams(continued)

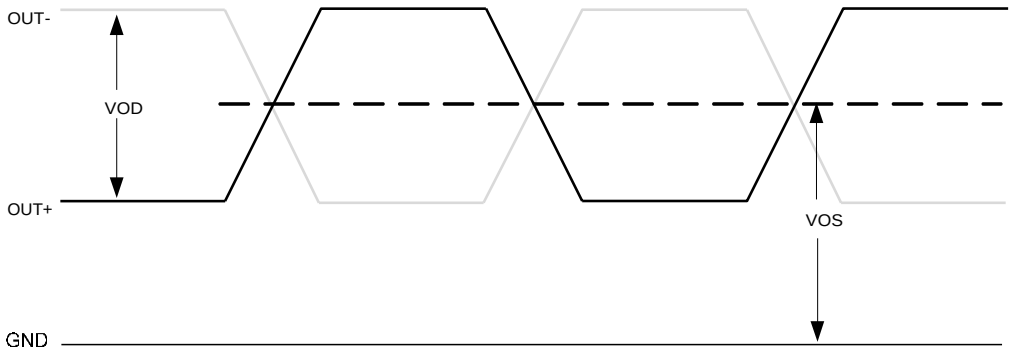


Figure 5. LVDS Voltage Levels per Differential Pin (OUT+/OUT-)

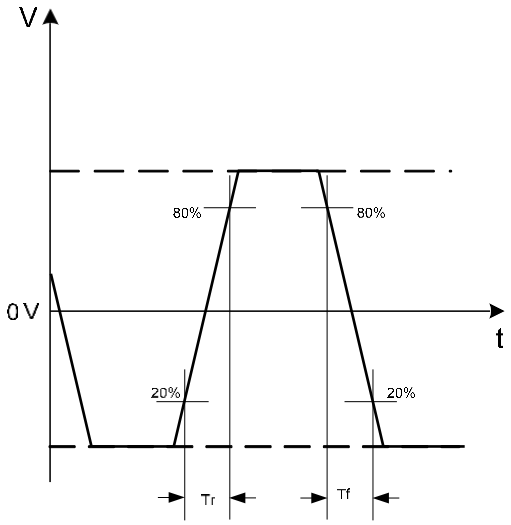


Figure 6. LVDS Differential Waveform

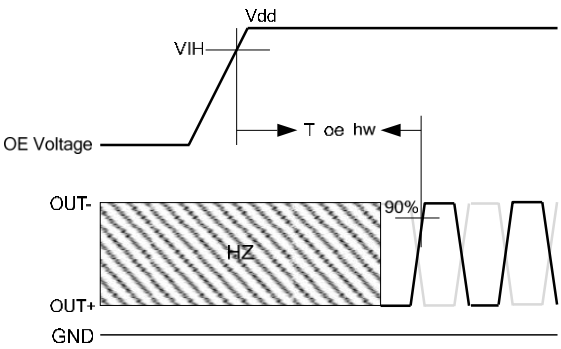


Figure 7. Hardware OE Enable Timing

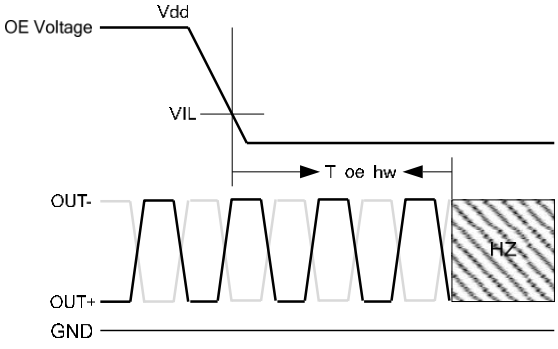


Figure 8. Hardware OE Disable Timing

Termination Diagrams

LVPECL:

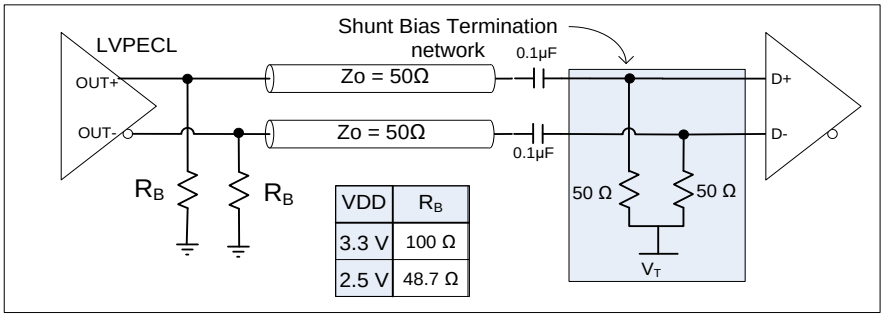


Figure 9. LVPECL with AC-coupled termination

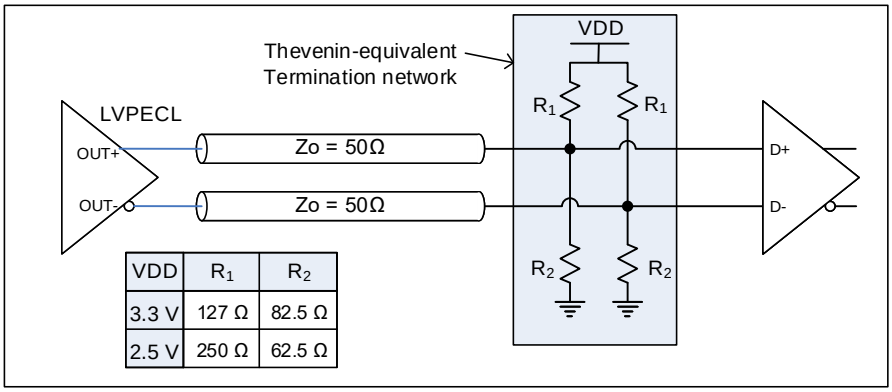


Figure 10. LVPECL DC-coupled load termination with Thevenin equivalent network

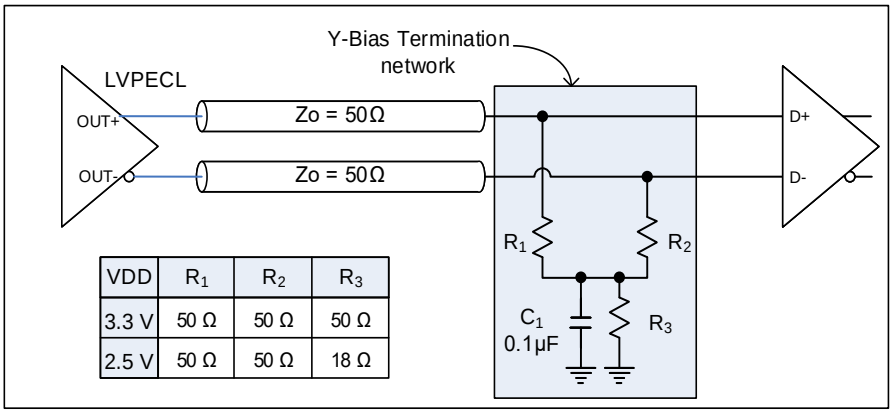


Figure 11. LVPECL with Y-Bias termination

Termination Diagrams (Continued)

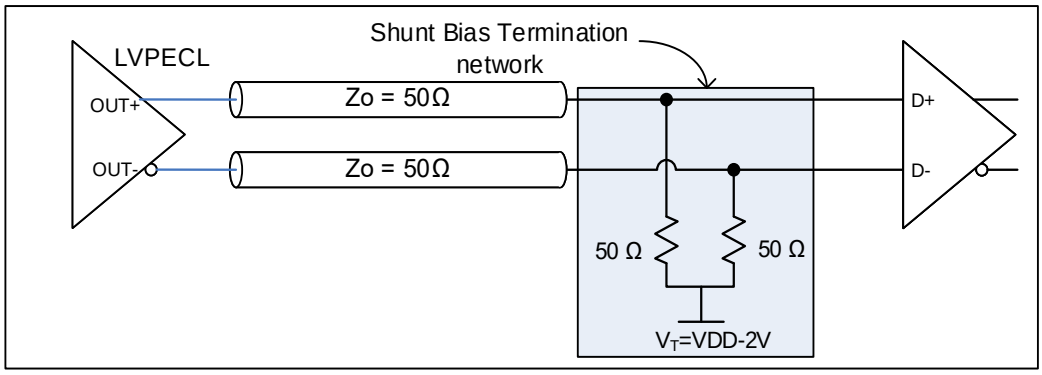


Figure 12. LVPECL with DC-coupled parallel shunt load termination

Termination Diagrams (Continued)

LVDS:

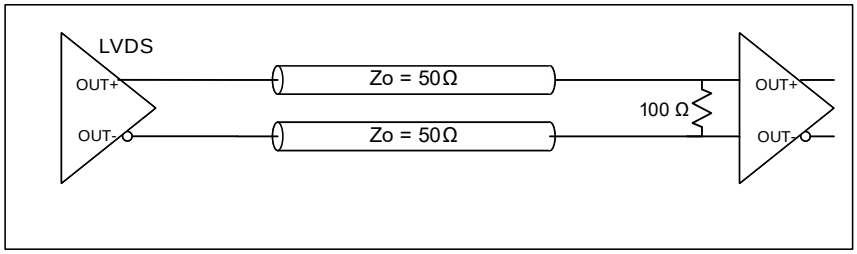


Figure 13. LVDS single DC termination at the load

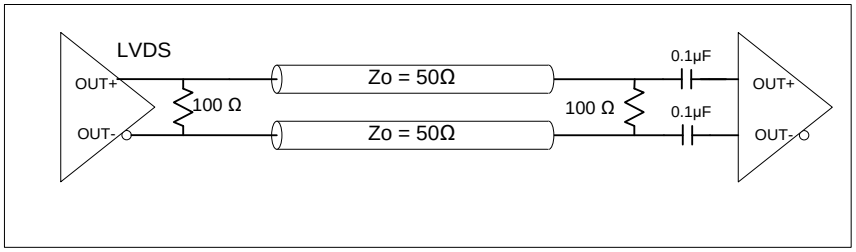


Figure 14. LVDS double AC termination with capacitor close to the load

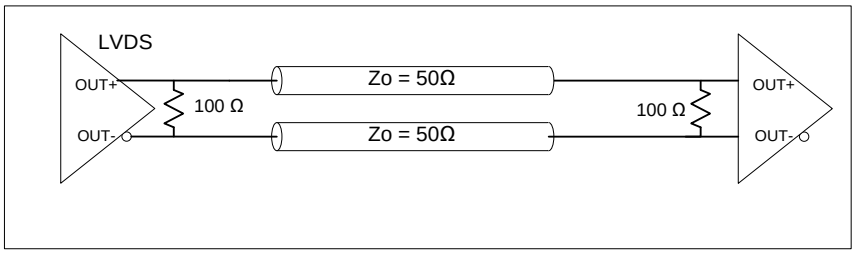


Figure 15. LVDS double DC termination

HCSL:

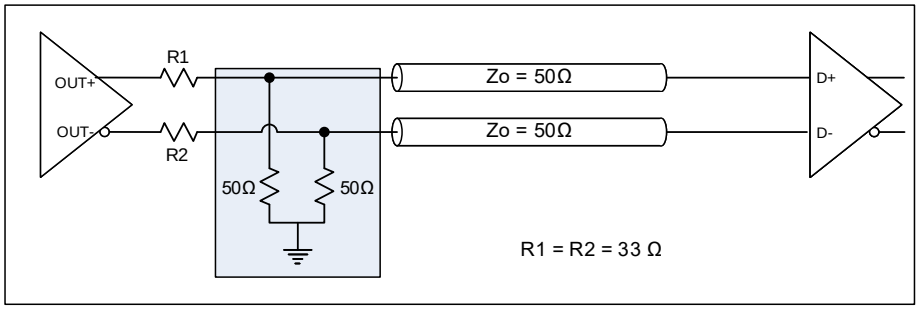
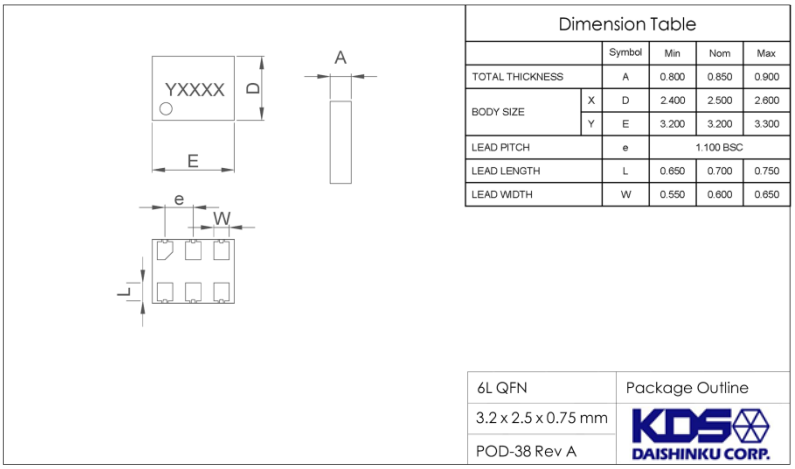


Figure 16. HCSL interface termination

Dimensions and Patterns

Package Size – Dimensions (Unit: mm)[9]	Recommended Land Pattern (Unit: mm)[10]

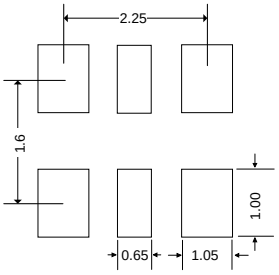
3.2 x 2.5x 0.85 mm



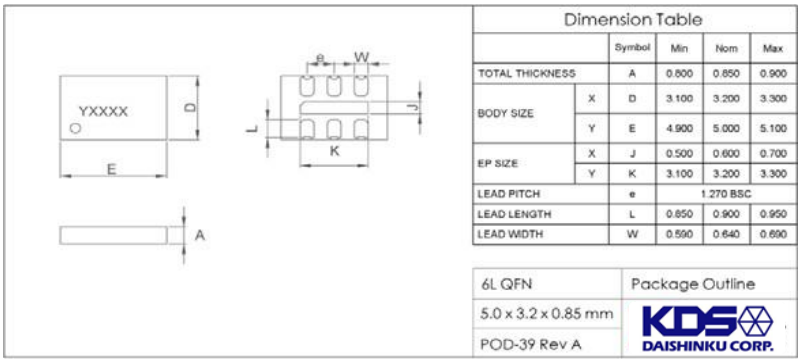
Dimension Table					
		Symbol	Min	Nom	Max
TOTAL THICKNESS		A	0.800	0.850	0.900
BODY SIZE	X	D	2.400	2.500	2.600
	Y	E	3.200	3.200	3.300
LEAD PITCH		e		1.100 BSC	
LEAD LENGTH		L	0.650	0.700	0.750
LEAD WIDTH		W	0.550	0.600	0.650

6L QFN	Package Outline
3.2 x 2.5 x 0.75 mm	KDS DAISHINKU CORP.
POD-38 Rev A	

3.2 x 2.5x 0.85 mm



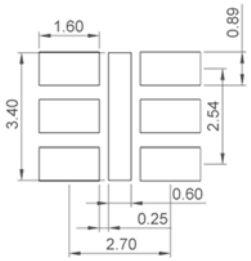
5.0 x 3.2x 0.85 mm[11]



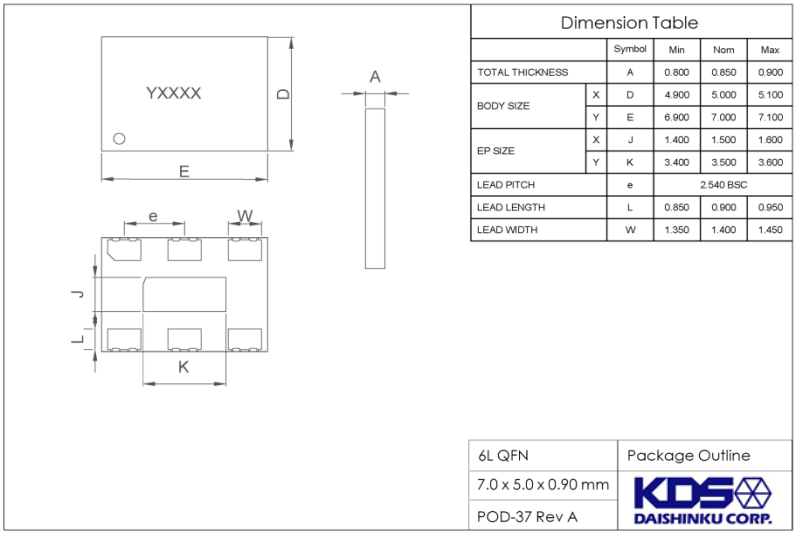
Dimension Table					
		Symbol	Min	Nom	Max
TOTAL THICKNESS		A	0.800	0.850	0.900
BODY SIZE	X	D	3.100	3.200	3.300
	Y	E	4.900	5.000	5.100
EP SIZE	X	J	0.500	0.600	0.700
	Y	K	3.100	3.200	3.300
LEAD PITCH		e		1.270 BSC	
LEAD LENGTH		L	0.850	0.900	0.950
LEAD WIDTH		W	0.590	0.640	0.690

6L QFN	Package Outline
5.0 x 3.2 x 0.85 mm	KDS DAISHINKU CORP.
POD-39 Rev A	

5.0 x 3.2 x 0.85 mm[11]



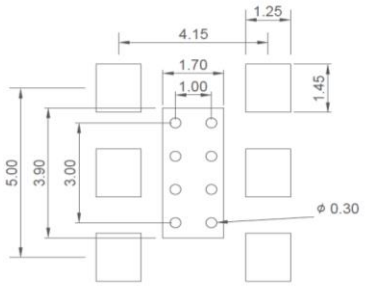
7.0 x 5.0x 0.85 mm[11]



Dimension Table					
		Symbol	Min	Nom	Max
TOTAL THICKNESS		A	0.800	0.850	0.900
BODY SIZE	X	D	4.900	5.000	5.100
	Y	E	6.900	7.000	7.100
EP SIZE	X	J	1.400	1.500	1.600
	Y	K	3.400	3.500	3.600
LEAD PITCH		e		2.540 BSC	
LEAD LENGTH		L	0.850	0.900	0.950
LEAD WIDTH		W	1.350	1.400	1.450

6L QFN	Package Outline
7.0 x 5.0 x 0.90 mm	KDS DAISHINKU CORP.
POD-37 Rev A	

7.0 x 5.0x 0.85 mm[11]



Note:
Circles in center pad are thermal vias, recommended to improve thermal performance

Notes:

9. Top Marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
10. A capacitor of value 0.1 µF or higher between Vdd and GND is required. An additional 10 µF capacitor between Vdd and GND is required for the best phase jitter performance
11. The center pad has no electrical function. Soldering down the center pad to the GND is recommended for best thermal dissipation, but is optional.

Ordering Information

M O 3 3 7 3 D B 6 - B 0 H - 3 3 N P - 0 2 2 0 1 2 3 4 5 6 D

Part Family
"MO3373"

Tempeature Range
"D" Extended Commercial -20ºC to +70ºC
"I" Industrial -40ºC to +85ºC
"J" -40ºC to +95ºC
"E" Extended Industrial -40ºC to +105ºC

Package Size
"D6" 3.2 x 2.5 mm
"B7" 5.0 x 3.2 mm with center pad
"A7" 7.0 x 5.0 mm with center pad

Signaling Type
"B" LVPECL
"D" LVDS
"H" HCSL

Signaling Function
"0" Default

Frequency Stability
"P" ±15 ppm[12]
"H" ±25 ppm
"J" ±35 ppm
"K" ±50 ppm

Packing
"Y","D" or "E"
Refer to table below for packing method

Frequency
220.000001 to 725.000000 MHz
cf.) 220.000001 MHz -> "0220000001"
725.000000 MHz -> "0725000000"

Pull Range Options[13]
"F" ±25 ppm
"H" ±50 ppm
"K" ±80 ppm
"L" ±100 ppm
"N" ±150 ppm
"P" ±200 ppm
"R" ±400 ppm
"S" ±800 ppm
"T" ±1600 ppm
"U" ±3200 ppm

Feature Pin[14]
"N" No Connect
"E" Output Enable (5.0x3.2, 7.0x5.0 mm only)

Supply Voltage
"25" +2.5 V ±10%
"28" +2.8 V ±10%
"30" +3.0 V ±10%
"33" +3.3 V ±10%

Notes:

12. Contact KDS for ±15 ppm
13. Contact KDS for custom pull range options
14. "E": Output Enable function is only available in 7.0 x 5.0 mm and 5.0 x 3.2 mm packages

Table 10. Ordering Codes for Supported Tape & Reel Packing Method

Device Size (mm x mm)	8 mm T&R (3ku)	8 mm T&R (1ku)	12 mm T&R (3ku)	12 mm T&R (1ku)	16 mm T&R (3ku)	16 mm T&R (1ku)
7.0 x 5.0 mm	–	–	–	–	–	Y
5.0 x 3.2 mm			–	Y	–	–
3.2 x 2.5 mm	D	E	–	–	–	–

Table 11. APR Table

Absolute pull range (APR) = Nominal pull range (PR) - frequency stability (F_stab)-aging

Nominal Pull Range	Frequency Stability			
	± 15	± 25	± 35	± 50
	APR (ppm)			
± 25	± 5	–	–	–
± 50	± 30	± 20	± 10	–
± 80	± 60	± 50	± 40	± 25
± 100	± 80	± 70	± 60	± 45
± 150	± 130	± 120	± 110	± 95
± 200	± 180	± 170	± 160	± 145
± 400	± 380	± 370	± 360	± 345
± 800	± 780	± 770	± 760	± 745
± 1600	± 1580	± 1570	± 1560	± 1545
± 3200	± 3180	± 3170	± 3160	± 3145

Table 12. Revision History

Revision	Release Date	Change Summary
1.0	10/13/2017	Initial release
1.03	05/10/2018	Updated the Part Ordering info with added 5.0 x 3.2 mm package