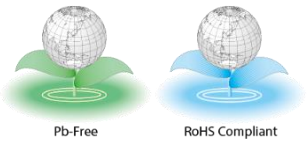
MO3808
1 MHz to 80 MHz High Performance VCMO

Features

- Any frequency between 1 and 80 MHz accurate to 6 decimal places of accuracy
- 100% pin-to-pin drop-in replacement to quartz-based VCXO
- Frequency stability as low as ±10 ppm
- Widest pull range options from ±25 ppm to ±1600 ppm
- Industrial or extended commercial temperature range
- Superior pull range linearity of ≤1%, 10 times better than quartz
- LVCMOS/LVTTL compatible output
- Four industry-standard packages:
  2.7 x 2.4 mm (4-pin) (compatible with 2.5 x 2.0 mm footprint),
  3.2 x 2.5mm (4-pin), 5.0 x 3.2 mm (6-pin), 7.0 x 5.0 mm (6-pin)
- Instant samples with Time Machine II and field programmable oscillators
- RoHS and REACH compliant, Pb-free, Halogen-free and Antimony-free

Applications

- Telecom clock synchronization, instrumentation
- Low bandwidth analog PLL, jitter cleaner, clock recovery, audio
- Video, 3G/HD-SDI, FPGA, broadband and networking



Electrical Specifications

Table 1. Electrical Characteristics[1,2,3]

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Range						
Output Frequency Range	f	1	–	80	MHz	
Frequency Stability and Aging						
Frequency Stability	F_stab	-10	–	+10	PPM	Inclusive of Initial tolerance[4] at +25 °C, and variations over operating temperature, rated power supply voltage and load
		-25	–	+25	PPM	
		-50	–	+50	PPM	
Aging	F_aging	-5	–	+5	PPM	10 years, +25°C
Operating Temperature Range	T_use	-20	–	+70	°C	Extended Commercial
		-40	–	+85	°C	Industrial
Supply Voltage and Current Consumption						
Supply Voltage	Vdd	+1.71	+1.8	+1.89	V	Supply voltages between +2.5V and +3.3V can be supported. Contact KDS for additional information.
		+2.25	+2.5	+2.75	V	
		+2.52	+2.8	+3.08	V	
		+2.97	+3.3	+3.63	V	
Current Consumption	Idd	–	+31	+33	mA	No load condition, f = 20 MHz, Vdd = +2.5V, +2.8V or +3.3V
		–	+29	+31	mA	No load condition, f = 20 MHz, Vdd = +1.8V
Standby Current	I_std	–	–	+70	µA	Vdd = +2.5V, +2.8V or +3.3V, $\overline{ST}$ = GND, output is Weakly Pulled Down
		–	–	+10	µA	Vdd = +1.8 V. $\overline{ST}$ = GND, output is Weakly Pulled Down
VCMO Characteristics						
Pull Range[5,6]	PR	±25, ±50, ±100, ±150, ±200, ±400, ±800, ±1600,			ppm	See the Absolute Pull Range and APR table on page 10
Upper Control Voltage	VC_U	+1.7	–	–	V	Vdd = +1.8V, Voltage at which maximum deviation is guaranteed.
		+2.4	–	–	V	Vdd = +2.5V, Voltage at which maximum deviation is guaranteed.
		+2.7	–	–	V	Vdd = +2.8V, Voltage at which maximum deviation is guaranteed.
		+3.2	–	–	V	Vdd = +3.3V, Voltage at which maximum deviation is guaranteed.
Lower Control Voltage	VC_L	–	–	+0.1	V	Voltage at which minimum deviation is guaranteed.
Control Voltage Input Impedance	Z_in	100	–	–	kΩ	
Control Voltage Input Capacitance	C_in	–	5	–	pF	
Linearity	Lin	–	0.1	1	%	
Frequency Change Polarity	–	Positive Slope			–	
Control Voltage Bandwidth (-3dB)	V_BW	–	8	–	kHz	Contact KDS for 16 kHz and other high bandwidth options

Electrical Specifications (continued)

Table 1. Electrical Characteristics[1,2,3]

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
LVCMOS Output Characteristics						
Duty Cycle	DC	45	–	55	%	All Vdds. Refer to Note 11 for definition of Duty Cycle
Rise/Fall Time	Tr,Tf	–	1.5	2.0	ns	Vdd = +1.8V, +2.5V, +2.8V or +3.3V, 10% - 90% Vdd level
Output High Voltage	VOH	90%	–	–	Vdd	IOH = -7 mA (Vdd = +3.0V or +3.3V) IOH = -4 mA (Vdd = +2.8V or +2.5V) IOH = -2 mA (Vdd = +1.8V)
Output Low Voltage	VOL	–	–	10%	Vdd	IOH = +7 mA (Vdd = +3.0V or +3.3V) IOH = +4 mA (Vdd = +2.8V or +2.5V) IOH = +2 mA (Vdd = +1.8V)
Input Characteristics						
Input Pull-up Impedance	Z_in	–	100	250	kΩ	For the OE/$\overline{ST}$ pin for 6-pin devices
Input Capacitance	C_in	–	5	–	pF	For the OE/$\overline{ST}$ pin for 6-pin devices
Startup and Resume Timing						
Startup Time	T_start	–	–	10	ms	See Figure 7 for startup resume timing diagram
OE Enable/Disable Time	T_oe	–	–	180	ns	f = 40 MHz, all Vdds. For other freq, T_oe = 100 ns + 3 clock periods
Resume Time	T_resume	–	7	10	ms	See Figure 8 for resume timing diagram
Jitter						
RMS Period Jitter	T_jitt	–	1.5	2.0	ps	f = 20 MHz, Vdd = +2.5V, +2.8V or +3.3V
		–	2.0	3.0	ps	f = 20 MHz, Vdd = +1.8V
RMS Phase Jitter (random)	T_phj	–	0.5	1.0	ps	f = 20 MHz, Integration bandwidth = 12 kHz to 20 MHz, All Vdds

Note:

1. All electrical specifications in the above table are specified with 15 pF output load and for all Vdd(s) unless otherwise stated.
2. The typical value of any parameter in the Electrical Characteristics table is specified for the nominal value of the highest voltage option for that parameter and at +25°C temperature
3. All max and min specifications are guaranteed across rated voltage variations and operating temperature ranges, unless specified otherwise
4. Initial tolerance is measured at Vin = Vdd/2
5. Absolute Pull Range (APR) is defined as the guaranteed pull range over temperature and voltage.
6. APR = pull range (PR) - frequency stability (F_stab) - Aging (F_aging)

Table 2. Pin Description. 4-Pin Configuration (For 2.7 x 2.0 mm and 3.2 x 2.5 mm Packages)

Pin	Symbol	Functionality	
1	VIN	Input	0-Vdd: produces voltage dependent frequency change
2	GND	Power	Electrical ground
3	CLK	Output	Oscillator output
4	VDD	Power	Power supply voltage[7]

Notes:

7. A capacitor value of 0.1 µF between VDD and GND is recommended.

Top View

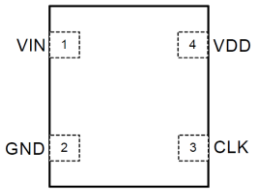


Figure 1.

Table 3. Pin Description. 6-Pin Configuration (For 5.0 x 3.2 mm and 7.0 x 5.0 mm Packages)

Pin	Symbol	Functionality	
1	VIN	Input	0-Vdd: produces voltage dependent frequency change
2	NC/OE/$\overline{ST}$	No Connect	H or L or Open: No effect on output frequency or other device function
		Output Enable	H or Open[8]: specified frequency output L: output is high
		Standby	H or Open[8]: specified frequency output L: output is low (weak pull down)[9]. Oscillation stops
3	GND	Power	Electrical ground
4	CLK	Output	Oscillator output
5	NC	No Connect	H or L or Open: No effect on output frequency or other device functions
6	VDD	Power	Power supply voltage[10]

Notes:

8. In OE or ST mode, a pull-up resistor of 10 kΩ or less is recommended if pin 2 in the 6-pin package is not externally driven. If pin 2 needs to be left floating, use the NC option.
9. Typical value of the weak pull-down impedance is 5 mΩ
10. A capacitor value of 0.1 µF between VDD and GND is recommended.

Top View

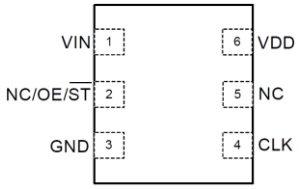


Figure 2.

Table 4. Absolute Maximum Limits

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	+150	°C
VDD	-0.5	+4.0	V
Electrostatic Discharge	–	+2000	V
Soldering Temperature (follow standard Pb free soldering guidelines)	–	+260	°C

Table 5. Thermal Consideration

Package	θJA, 4 Layer Board (°C/W)	θJA, 2 Layer Board (°C/W)	θJC, Bottom (°C/W)
7050	191	263	30
5032	97	199	24
3225	109	212	27
2724	117	222	26

Table 6. Environmental Compliance

Parameter	Condition/Test Method
Mechanical Shock	**MIL-STD-883F, Method 2002**
Mechanical Vibration	**MIL-STD-883F, Method 2007**
Temperature Cycle	**JESD22, Method A104**
Solderability	**MIL-STD-883F, Method 2003**
Moisture Sensitivity Level	**MSL1 @ 260°C**

Phase Noise Plot

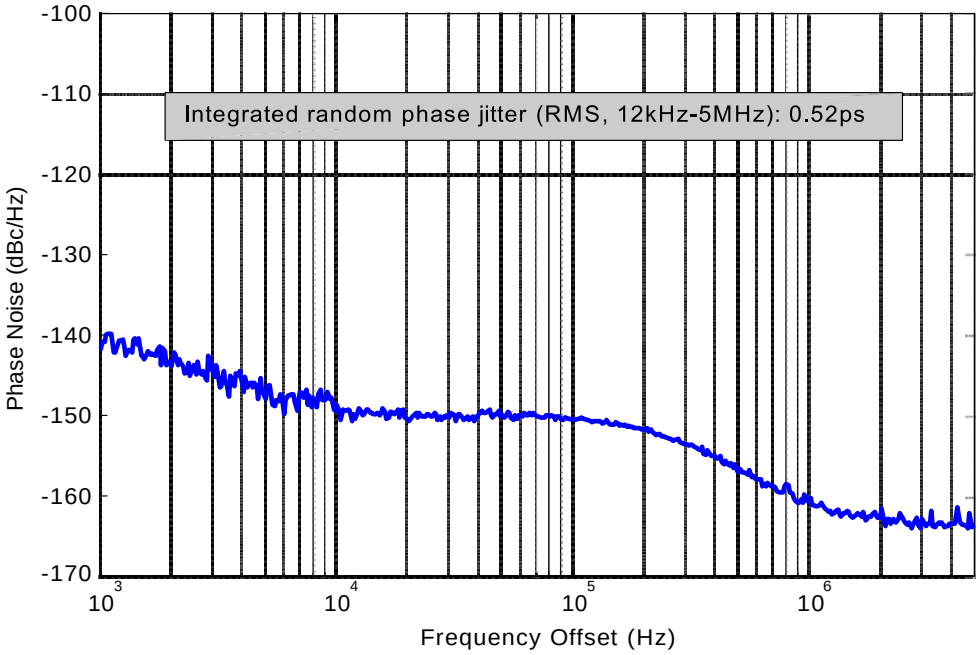


Figure 3. Phase Noise, 10 MHz, +3.3V, LVCMOS Output

Test Circuit and Waveform

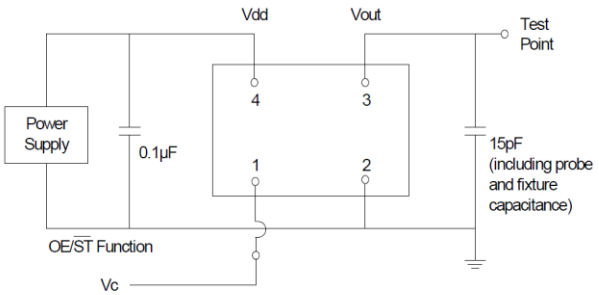


Figure 4. Test Circuit (4-Pin Device)

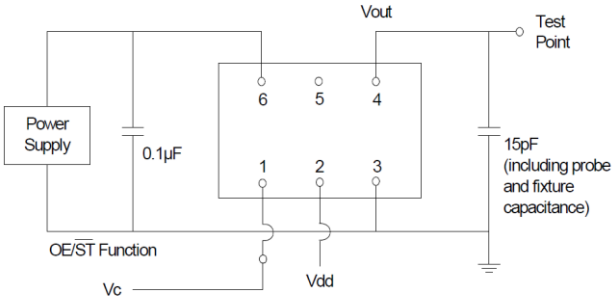


Figure 5. Test Circuit (6-Pin Device)

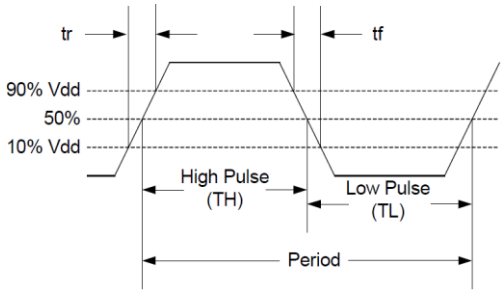


Figure 6. Waveform

Notes:

11. Duty Cycle is computed as Duty Cycle = TH/Period.
12. MO3808 supports the configurable duty cycle feature. For custom duty cycle at any given frequency, contact KDS.

Timing Diagram

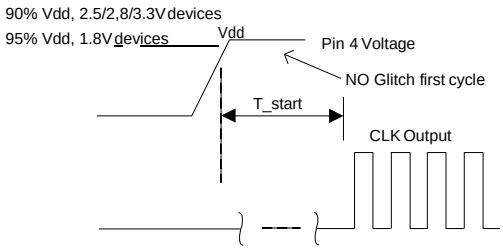


Figure 7. Startup Timing (OE/$\overline{ST}$ Mode)

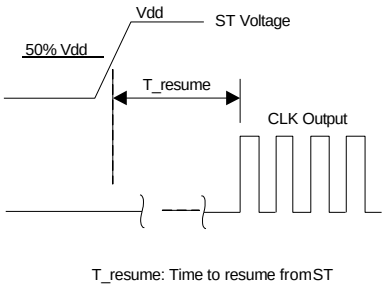


Figure 8. Standby Resume Timing ($\overline{ST}$ Mode Only)

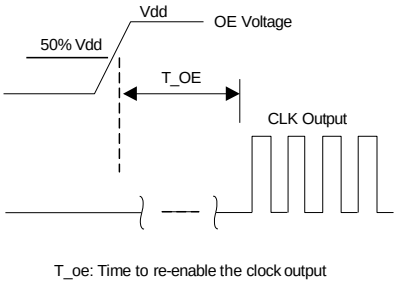


Figure 9. OE Enable Timing (OE Mode Only)

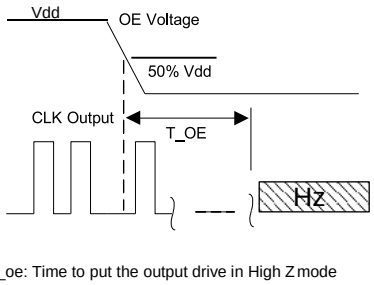


Figure 10. OE Disable Timing (OE Mode Only)

Notes:
13. MO3808 supports “no runt” pulses and “no glitch” output during startup or resume.
14. MO3808 supports gated output which is accurate within rated frequency stability from the first cycle.

Programmable Drive Strength

The MO3808 includes a programmable drive strength feature to provide a simple, flexible tool to optimize the clock rise/fall time for specific applications. Benefits from the programmable drive strength feature are:

- Improves system radiated electromagnetic interference (EMI) by slowing down the clock rise/fall time
- Improves the downstream clock receiver's (RX) jitter by decreasing (speeding up) the clock rise/fall time.
- Ability to drive large capacitive loads while maintaining full swing with sharp edge rates.

For more detailed information about rise/fall time control and drive strength selection, Contact KDS.

EMI Reduction by Slowing Rise/Fall Time

Figure 11 shows the harmonic power reduction as the rise/fall times are increased (slowed down). The rise/fall times are expressed as a ratio of the clock period. For the ratio of 0.05, the signal is very close to a square wave. For the ratio of 0.45, the signal is very close to near-triangular waveform. These results, for example, show that the 11th clock harmonic can be reduced by 35 dB if the rise/fall edge is increased from 5% of the period to 45% of the period.

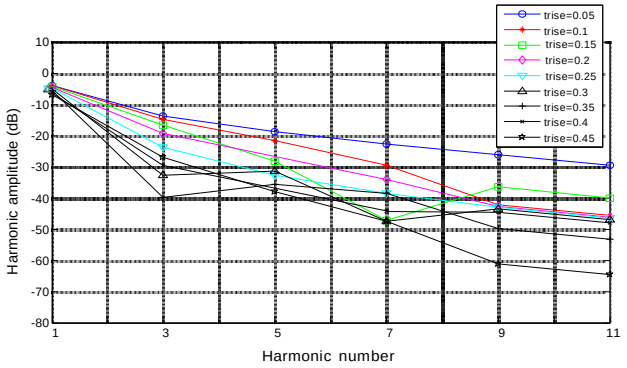


Figure 11. Harmonic EMI reduction as a Function of Slower Rise/Fall Time

Jitter Reduction with Faster Rise/Fall Time

Power supply noise can be a source of jitter for the downstream chipset. One way to reduce this jitter is to increase rise/fall time (edge rate) of the input clock. Some chipsets would require faster rise/fall time in order to reduce their sensitivity to this type of jitter. Refer to the Rise/Fall Time Tables to determine the proper drive strength.

High Output Load Capability

The rise/fall time of the input clock varies as a function of the actual capacitive load the clock drives. At any given drive strength, the rise/fall time becomes slower as the output load increases. As an example, for a +3.3V MO3808 device with default drive strength setting, the typical rise/fall time is 1.15ns for 15 pF output load. The typical rise/fall time slows down to 2.72ns when the output load increases to 45 pF. One can choose to speed up the rise/fall time to 1.41ns by then increasing the drive strength setting on the MO3808.

The MO3808 can support up to 60 pF maximum capacitive loads. Refer to the Rise/Tall Time Tables to determine the proper drive strength for the desired combination of output load vs. rise/fall time

MO3808 Drive Strength Selection

Tables 7 through 10 define the rise/fall time for a given capac- itive load and supply voltage.

1. Select the table that matches the MO3808 nominal supply voltage (+1.8V, +2.5V, +2.8V, +3.0V, +3.3V).
2. Select the capacitive load column that matches the application requirement (5 pF to 60 pF)
3. Under the capacitive load column, select the desired rise/fall times.
4. The left-most column represents the part number code for the corresponding drive strength.
5. Add the drive strength code to the part number for ordering purposes.

Calculating Maximum Frequency

Based on the rise and fall time data given in Tables 7 through 10, the maximum frequency the oscillator can operate with guaranteed full swing of the output voltage over temperature as follows:

$$\text{Max Frequency} = \frac{1}{6 \times Trf\_10/90}$$

Where Trf_10/90 is the typical rise/fall time at 10% to 90% Vdd.

Example 1

Calculate f_{MAX} for the following condition:

- Vdd = +3.3V (Table 10)
- Capacitive Load: 30 pF
- Typical Tr/f time = 1.66 ns (rise/fall time part number code =G)

Part number for the above example:

MO3808ID4-C**G**H-33NP-0049152000

Drive strength code is here.

Rise/Fall Time (10% to 90%) vs C_{LOAD} Tables

Table 7. Vdd = +1.8V Rise/Fall Times for Specific C_{LOAD}

Rise/Fall Time Typ (ns)					
Drive Strength \ C_{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF
L	12.45	17.68	19.48	46.21	57.82
A	6.50	10.27	16.21	23.92	30.73
R	4.38	7.05	11.61	16.17	20.83
B	3.27	5.30	8.89	12.18	15.75
S	2.62	4.25	7.20	9.81	12.65
D	2.19	3.52	6.00	8.31	10.59
T	1.76	3.01	5.14	7.10	9.15
E	1.59	2.59	4.49	6.25	7.98
U	1.49	2.28	3.96	5.55	7.15
F	1.22	2.10	3.57	5.00	6.46
W	1.07	1.88	3.23	4.50	5.87
G	1.01	1.64	2.95	4.12	5.40
X	0.96	1.50	2.74	3.80	4.98
K	0.92	1.41	2.56	3.52	4.64
Y	0.88	1.34	2.39	3.25	4.32
Q	0.86	1.29	2.24	3.04	4.06
Z or "0": Default	0.82	1.24	2.07	2.89	3.82
M	0.77	1.20	1.94	2.72	3.61
N	0.66	1.15	1.84	2.58	3.41
P	0.51	1.09	1.76	2.45	3.24

Table 8. Vdd = +2.5V Rise/Fall Times for Specific C_{LOAD}

Rise/Fall Time Typ (ns)					
Drive Strength \ C_{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF
L	8.68	13.59	18.36	32.70	42.06
A	4.42	7.18	11.93	16.60	21.38
R	2.93	4.78	8.15	11.19	14.59
B	2.21	3.57	6.19	8.55	11.04
S	1.67	2.87	4.94	6.85	8.80
D	1.50	2.33	4.11	5.68	7.33
T	1.06	2.04	3.50	4.84	6.26
E	0.98	1.69	3.03	4.20	5.51
U	0.93	1.48	2.69	3.73	4.92
F	0.90	1.37	2.44	3.34	4.42
W	0.87	1.29	2.21	3.04	4.02
G or "0": Default	0.67	1.20	2.00	2.79	3.69
X	0.44	1.10	1.86	2.56	3.43
K	0.38	0.99	1.76	2.37	3.18
Y	0.36	0.83	1.66	2.20	2.98
Q	0.34	0.71	1.58	2.07	2.80
Z	0.33	0.65	1.51	1.95	2.65
M	0.32	0.62	1.44	1.85	2.50
N	0.31	0.59	1.37	1.77	2.39
P	0.30	0.57	1.29	1.70	2.28

Table 9. Vdd = +2.8V Rise/Fall Times for Specific C_{LOAD}

Rise/Fall Time Typ (ns)					
Drive Strength \ C_{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF
L	7.93	12.69	17.94	30.10	38.89
A	4.06	6.66	11.04	15.31	19.80
R	2.68	4.40	7.53	10.29	13.37
B	2.00	3.25	5.66	7.84	10.11
S	1.59	2.57	4.54	6.27	8.07
D	1.19	2.14	3.76	5.21	6.72
T	1.00	1.79	3.20	4.43	5.77
E	0.94	1.51	2.78	3.84	5.06
U	0.90	1.38	2.48	3.40	4.50
F	0.87	1.29	2.21	3.03	4.05
W	0.62	1.19	1.99	2.76	3.68
G or "0": Default	0.41	1.08	1.84	2.52	3.36
X	0.37	0.96	1.72	2.33	3.15
K	0.35	0.78	1.63	2.15	2.92
Y	0.33	0.67	1.54	2.00	2.75
Q	0.32	0.63	1.46	1.89	2.57
Z	0.31	0.60	1.39	1.80	2.43
M	0.30	0.57	1.31	1.72	2.30
N	0.30	0.56	1.22	1.63	2.22
P	0.29	0.54	1.13	1.55	2.13

Table 10. Vdd = +3.3V Rise/Fall Times for Specific C_{LOAD}

Rise/Fall Time Typ (ns)					
Drive Strength \ C_{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF
L	7.18	11.59	17.24	27.57	35.57
A	3.61	6.02	10.19	13.98	18.10
R	2.31	3.95	6.88	9.42	12.24
B	1.65	2.92	5.12	7.10	9.17
S	1.43	2.26	4.09	5.66	7.34
D	1.01	1.91	3.38	4.69	6.14
T	0.94	1.51	2.86	3.97	5.25
E	0.90	1.36	2.50	3.46	4.58
U	0.86	1.25	2.21	3.03	4.07
F or "0": Default	0.48	1.15	1.95	2.72	3.65
W	0.38	1.04	1.77	2.47	3.31
G	0.36	0.87	1.66	2.23	3.03
X	0.34	0.70	1.56	2.04	2.80
K	0.33	0.63	1.48	1.89	2.61
Y	0.32	0.60	1.40	1.79	2.43
Q	0.32	0.58	1.31	1.69	2.28
Z	0.30	0.56	1.22	1.62	2.17
M	0.30	0.55	1.12	1.54	2.07
N	0.30	0.54	1.02	1.47	1.97
P	0.29	0.52	0.95	1.41	1.90

Instant Samples with Time Machine and Field Programmable Oscillators

KDS supports a field programmable version of the MO3808 low power oscillator for fast prototyping and real time customization of features. The field programmable devices (FP devices) are available for all four standard MO3808 package sizes and can be configured to one's exact specification using the Time Machine II, an USB powered MEMS oscillator programmer.

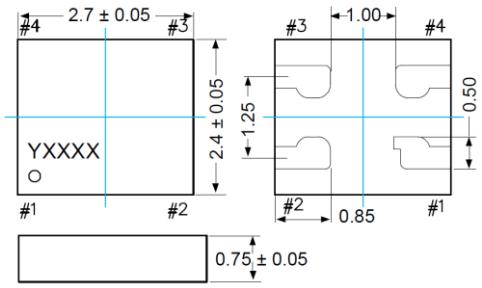
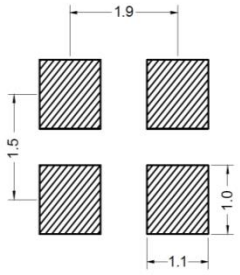
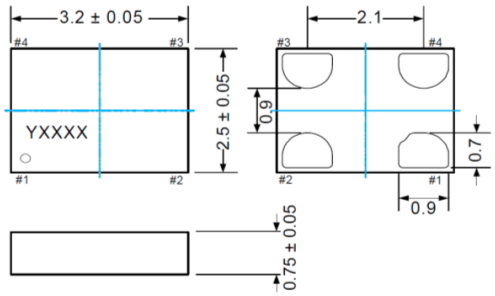
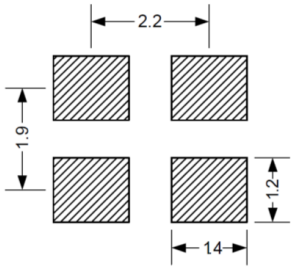
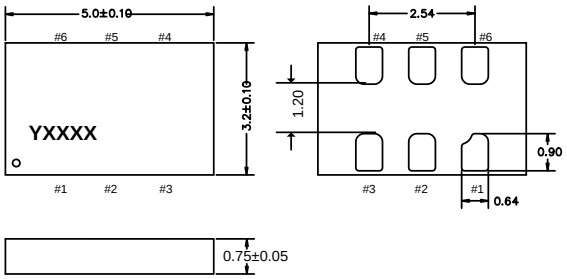
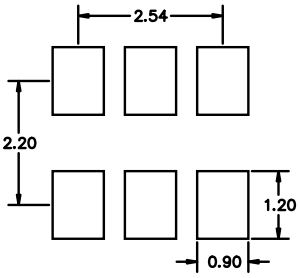
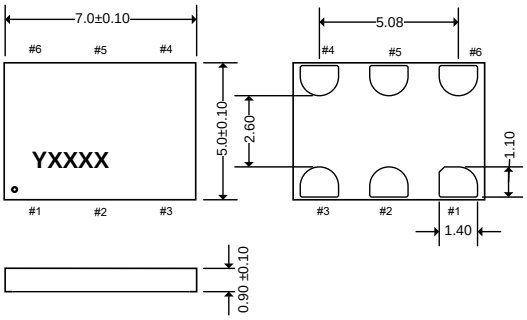
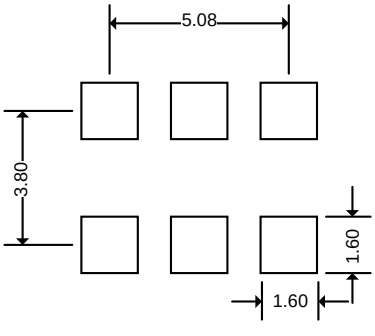
Customizable Features of the MO3808 FP Devices Include

- Any frequency between 1 – 80 MHz
- Three frequency stability options, ±10 ppm, ±25 ppm, ±50 ppm
- Two operating temperatures, -20 to +70°C or -40 to +85°C
- Four supply voltage options, +1.8V, +2.5V, +2.8V, +3.3V
- Eight pull range options: ±25 ppm, ±50 ppm, ±100 ppm, ±150 ppm, ±200 ppm, ±400 ppm, ±800 ppm, ±1600 ppm

For more information regarding KDS's field programmable solutions, contact KDS.

MO3808 is typically factory-programmed per customer ordering codes for volume delivery.

Dimensions and Patterns

Package Size – Dimensions (Unit: mm)[15]	Recommended Land Pattern (Unit: mm)
2.7 x 2.4 x 0.75 mm (100% compatible with 2.5 x 2. 0 mm footprint) 	
3.2 x 2.5 x 0.75 mm 	
5.0 x 3.2 x 0.75 mm 	
7.0 x 5.0x 0.90 mm 	

Notes:
15. Top marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.

Ordering Information

M O 3 8 0 8 D D 4 - C 0 H - 3 3 N P - 0 0 4 9 1 5 2 0 0 0 Y

Part Family
"MO3808"

Tempeature Range
"D" Extended Commercial -20ºC to +70ºC
"I" Industrial -40ºC to +85ºC

Package Size
"F4" 2.7 x 2.4 mm
(compatible with 2.5 x 2.0 mm footprint)
"D4" 4-pin 3.2 x 2.5 mm
"B6" 6-pin 5.0 x 3.2 mm
"A6" 6-pin 7.0 x 5.0 mm

Signaling Type
"C" LVCMOS

Output Drive Strength
See Table 7 to 10 for rise/fall times
"0": Default (datasheet limits)
"L" "S" "U" "X" "Z"
"A" "D" "F" "K" "M"
"R" "T" "W" "Y" "N"
"B" "E" "G" "Q" "P"

Frequency Stability
"F" ±10ppm
"H" ±25ppm
"K" ±50ppm

Packing
"Y" 12mm Tape & Reel, 1ku reel
"D" 8mm Tape & Reel, 3ku reel
"E" 8mm Tape & Reel, 1ku reel

Frequency
1.000000 to 80.000000MHz
cf.) 1.000000MHz -> "0001000000"
80.000000MHz -> "0080000000"

Pull Range Options
"F" ±25 ppm
"H" ±50 ppm
"L" ±100 ppm
"N" ±150 ppm
"P" ±200 ppm
"R" ±400 ppm
"S" ±800 ppm
"T" ±1600 ppm

Feature Pin
"E" Output Enable (6-pin only)
"S" Standby (6-pin only)
"N" No Connect in 6-pin devices
Default value in 4-pin devices

Supply Voltage
"18" +1.8V ±10%
"25" +2.5V ±10%
"28" +2.8V ±10%
"33" +3.3V ±10%

Table 12. APR Table

Absolute pull range (APR) = Nominal pull range (PR) – frequency stability (F_stab) – Aging (F_aging)

Nominal Pull Range	Frequency Stability		
	±10	±25	±50
	APR (ppm)		
±25	±10	-	-
±50	±35	±20	-
±100	±85	±70	±45
±150	±135	±120	±95
±200	±185	±170	±145
±400	±385	±370	±345
±800	±785	±770	±745
±1600	±1585	±1570	±1545

Table 13. Ordering Codes for Supported Tape & Reel Packing Method[16]

Device Size	12 mm T&R (3ku)	12 mm T&R (1ku)	8 mm T&R (3ku)	8 mm T&R (1ku)
2.7 x 2.4 mm	–	–	D	E
3.2 x 2.5 mm	–	–	D	E
5.0 x 3.2 mm	–	Y	–	–
7.0 x 5.0 mm	–	Y	–	–

Notes:
16. "-" indicates "not available."

Revision History

Table 14. Datasheet Version and Change Log

Version	Release Date	Change Summary
0.6	1/24/13	Preliminary
1.0	3/7/14	· Preliminary removed from title · Updated features and application · Updated electrical specifications table · Updated figure 4, · Added new 6-pin device for figure 5 · Updated timing diagrams · Updated programmable drive strength section · Updated ordering information drawing · Updated APR table · Updated ordering codes for tape and reel table · Reformatted additional information table columns
1.01	1/8/15	· Corrected CLK and VDD functionality description in Table 2 · Revised VIN functionality description in Table 3