

MO5021

1-220 MHz High Performance Differential (VC) TCXO

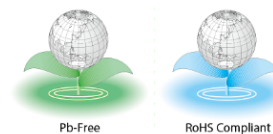


Feature

- Any frequency between 1 MHz and 220 MHz accurate to 6 decimal places
- LVPECL and LVDS output signaling types
- 0.6ps RMS phase jitter (random) over 12 kHz to 20 MHz bandwidth
- Frequency stability as low as ± 5 ppm. Contact KDS for tighter stability options
- Industrial and extended commercial temperature ranges
- Industry-standard packages: 3.2 x 2.5, 5.0 x 3.2 and 7.0 x 5.0 mm
- For frequencies higher than 220 MHz, refer to MO5022 datasheet

Applications

- SATA, SAS, 10GB Ethernet, Fibre Channel, PCI-Express
- Networking, broadband, instrumentation



Electrical Characteristics

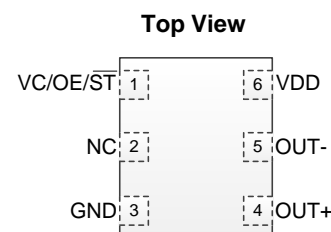
Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
LVPECL and LVDS, Common Electrical Characteristics						
Supply Voltage	V _{dd}	+2.97	+3.3	+3.63	V	
		+2.25	+2.5	+2.75	V	
		+2.25	–	+3.63	V	Termination schemes in Figures 1 and 2 - XX ordering code
Output Frequency Range	f	1	–	220	MHz	
Initial Tolerance	F _{init}	-2.0	–	2.0	ppm	At +25°C after two reflows
Stability Over Temperature	F _{stab}	-5.0	–	+5.0	ppm	Over operating temperature range at rated nominal power supply voltage and load. Contact KDS for tighter stability options.
Supply Voltage	F _{vdd}	–	+50	–	ppb	$\pm 10\%$ V _{dd}
Output Load	F _{load}	–	+0.1	–	ppm	15 pF $\pm 10\%$ of load
First Year Aging	F _{aging1}	-2.5	–	+2.5	ppm	+25°C
10-year Aging	F _{aging10}	-5.0	–	+5.0	ppm	+25°C
Operating Temperature Range	T _{use}	-40	–	+85	°C	Industrial
		-20	–	+70	°C	Extended Commercial
Pull Range	PR	$\pm 12.5, \pm 25, \pm 50$			ppm	
Upper Control Voltage	VC _U	V _{dd} -0.1	–	–	V	All V _{dds} . Voltage at which maximum deviation is guaranteed.
Control Voltage Range	VC _L	–	–	+0.1	V	
Control Voltage Input Impedance	Z _{vc}	100	–	–	k Ω	
Frequency Change Polarity	–	Positive slope			–	
Control Voltage -3dB Bandwidth	V _{BW}	–	–	8	kHz	
Input Voltage High	V _{IH}	70%	–	–	V _{dd}	Pin 1, OE or \overline{ST}
Input Voltage Low	V _{IL}	–	–	30%	V _{dd}	Pin 1, OE or \overline{ST}
Input Pull-up Impedance	Z _{in}	–	100	250	k Ω	Pin 1, OE logic high or logic low, or \overline{ST} logic high
		2.0	–	–	M Ω	Pin 1, \overline{ST} logic low
Start-up Time	T _{start}	–	6.0	10	ms	Measured from the time V _{dd} reaches its rated minimum value.
Resume Time	T _{resume}	–	6.0	10	ms	In Standby mode, measured from the time \overline{ST} pin crosses
Duty Cycle	DC	45	–	55	%	Contact KDS for tighter duty cycle
LVPECL, DC and AC Characteristics						
Current Consumption	I _{dd}	–	+61	+69	mA	Excluding Load Termination Current, V _{dd} = +3.3V or +2.5V
OE Disable Supply Current	I _{OE}	–	–	+35	mA	OE = Low
Output Disable Leakage Current	I _{leak}	–	–	+1.0	μ A	OE = Low
Standby Current	I _{std}	–	–	+100	μ A	\overline{ST} = Low, for all V _{dds}
Maximum Output Current	I _{driver}	–	–	+30	mA	Maximum average current drawn from OUT+ or OUT-
Output High Voltage	VOH	V _{dd} -1.1	–	V _{dd} -0.7	V	See Figure 1(a)
Output Low Voltage	VOL	V _{dd} -1.9	–	V _{dd} -1.5	V	See Figure 1(a)
Output Differential Voltage Swing	V _{Swing}	+1.2	+1.6	+2.0	V	See Figure 1(b)
Rise/Fall Time	T _r , T _f	–	300	500	ps	20% to 80%, see Figure 1(a)
OE Enable/Disable Time	T _{oe}	–	–	115	ns	f = 212.5 MHz - For other frequencies, T _{oe} = 100ns + 3 period
RMS Period Jitter	T _{jitt}	–	1.2	1.7	ps	f = 100 MHz, V _{DD} = +3.3V or +2.5V
		–	1.2	1.7	ps	f = 156.25 MHz, V _{DD} = +3.3V or +2.5V
		–	1.2	1.7	ps	f = 212.5 MHz, V _{DD} = +3.3V or +2.5V
RMS Phase Jitter (random)	T _{phj}	–	0.6	0.85	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V _{dds}

Electrical Characteristics(continued)

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
LVDS, DC and AC Characteristics						
Current Consumption	I _{dd}	–	+47	+55	mA	Excluding Load Termination Current, V _{dd} = +3.3V or +2.5V
OE Disable Supply Current	I _{OE}	–	–	+35	mA	OE = Low
Differential Output Voltage	V _{OD}	+250	+350	+450	mV	See Figure 2
Output Disable Leakage Current	I _{leak}	–	–	+1.0	μA	OE = Low
Standby Current	I _{std}	–	–	+100	μA	\overline{ST} = Low, for all V _{dds}
VOD Magnitude Change	ΔV _{OD}	–	–	+50	mV	See Figure 2
Offset Voltage	V _{OS}	+1.125	+1.2	+1.375	V	See Figure 2
VOS Magnitude Change	ΔV _{OS}	–	–	+50	mV	See Figure 2
Rise/Fall Time	T _r , T _f	–	495	600	ps	20% to 80%, see Figure 2
OE Enable/Disable Time	T _{oe}	–	–	115	ns	f = 212.5 MHz - For other frequencies, T _{oe} = 100ns + 3 period
RMS Period Jitter	T _{jitt}	–	1.2	1.7	ps	f = 100 MHz, V _{DD} = +3.3V or +2.5V
		–	1.2	1.7	ps	f = 156.25 MHz, V _{DD} = +3.3V or +2.5V
		–	1.2	1.7	ps	f = 212.5 MHz, V _{DD} = +3.3V or +2.5V
RMS Phase Jitter (random)	T _{phj}	–	0.6	0.85	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V _{dds}

Pin Description

Pin	Map	Functionality	
1	VC / OE / \overline{ST}	V Control	Voltage control
		Output Enable	H or Open: specified frequency output L: output is high impedance
		Standby	H or Open: specified frequency output L: Device goes to sleep mode. Supply current reduces to I _{std} .
2	NC	NA	No Connect; Leave it floating or connect to GND for better heat dissipation
3	GND	Power	V _{DD} Power Supply Ground
4	OUT+	Output	Oscillator output
5	OUT-	Output	Complementary oscillator output
6	V _{DD}	Power	Power supply voltage



Absolute Maximum

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	+150	°C
V _{DD}	-0.5	+4.0	V
Electrostatic Discharge (HBM)	–	+2000	V
Soldering Temperature (follow standard Pb free soldering guidelines)	–	+260	°C

Thermal Consideration

Package	θ _{JA} , 4 Layer Board (°C/W)	θ _{JC} , Bottom (°C/W)
7050, 6-pin	142	27
5032, 6-pin	97	20
3225, 6-pin	109	20

Environmental Compliance

Parameter	Condition/Test Method
Mechanical Shock	MIL-STD-883F, Method2002
Mechanical Vibration	MIL-STD-883F, Method2007
Temperature Cycle	JESD22, Method A104
Solderability	MIL-STD-883F, Method2003
Moisture Sensitivity Level	MSL1 @ +260°C

Waveform Diagrams

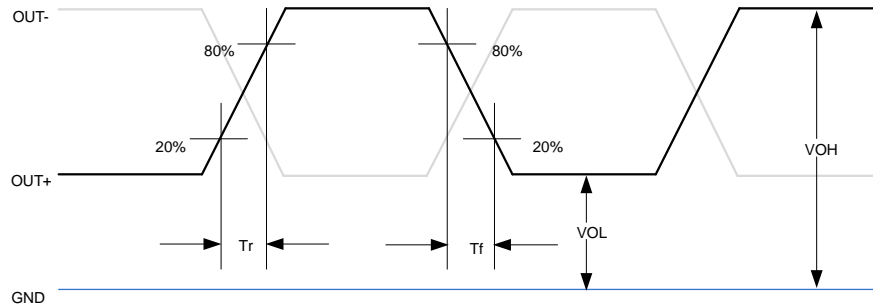


Figure 1(a). LVPECL Voltage Levels per Differential Pin (OUT+/OUT-)

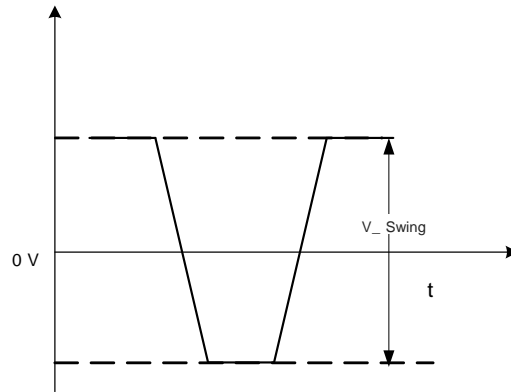


Figure 1(b). LVPECL Voltage Levels across Differential Pair

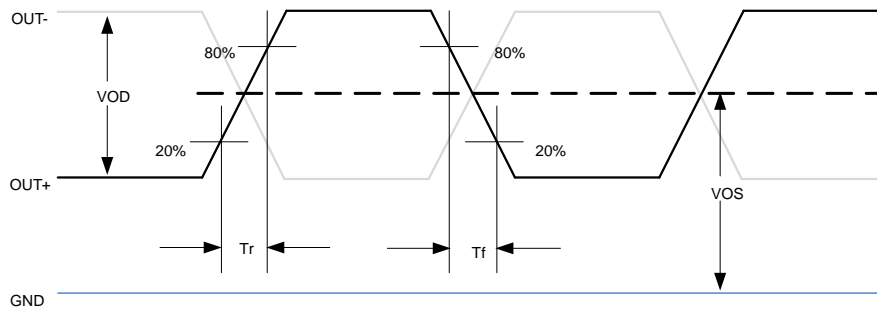


Figure 2. LVDS Voltage Levels per Differential Pin (OUT+/OUT-)

Termination Diagrams

LVPECL:

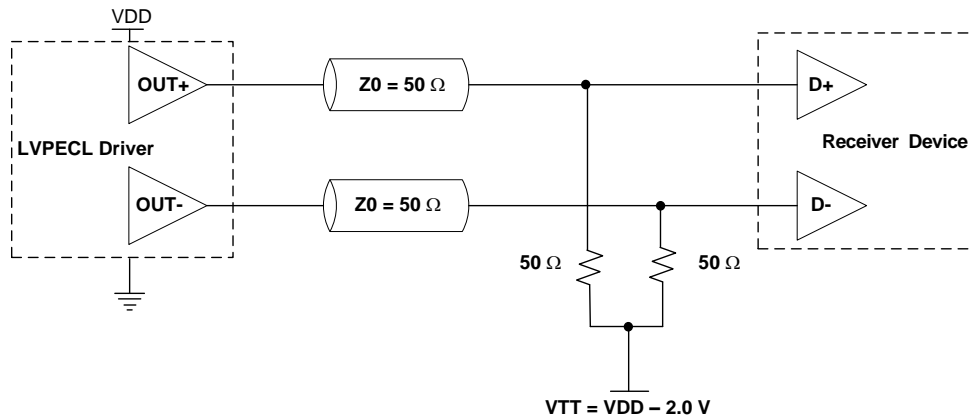


Figure 3. LVPECL Typical Termination

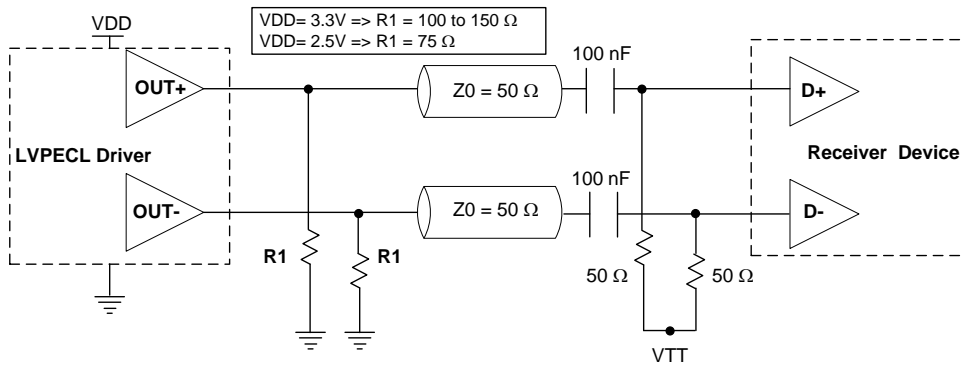


Figure 4. LVPECL AC Coupled Termination

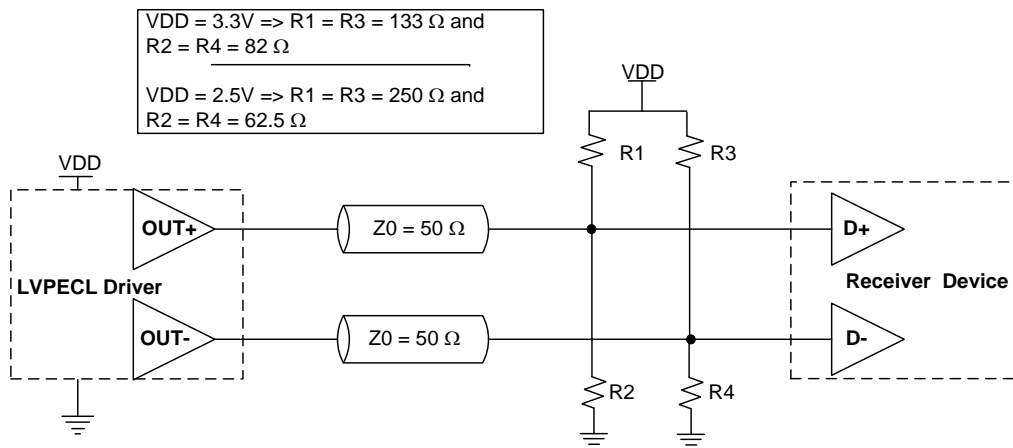


Figure 5. LVPECL with Thevenin Typical Termination

LVDS:

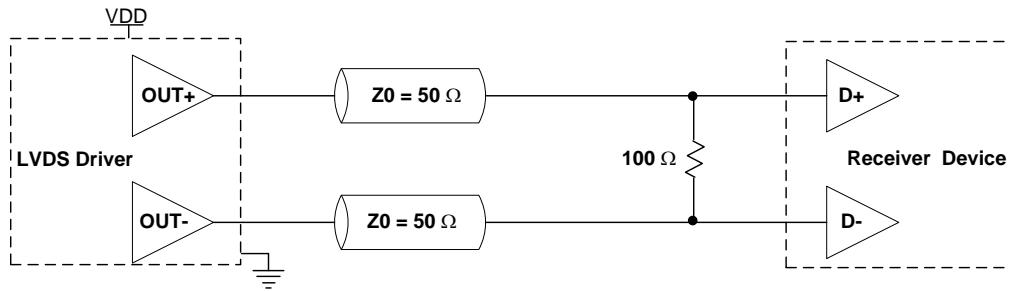


Figure 6. LVDS Single Termination (Load Terminated)

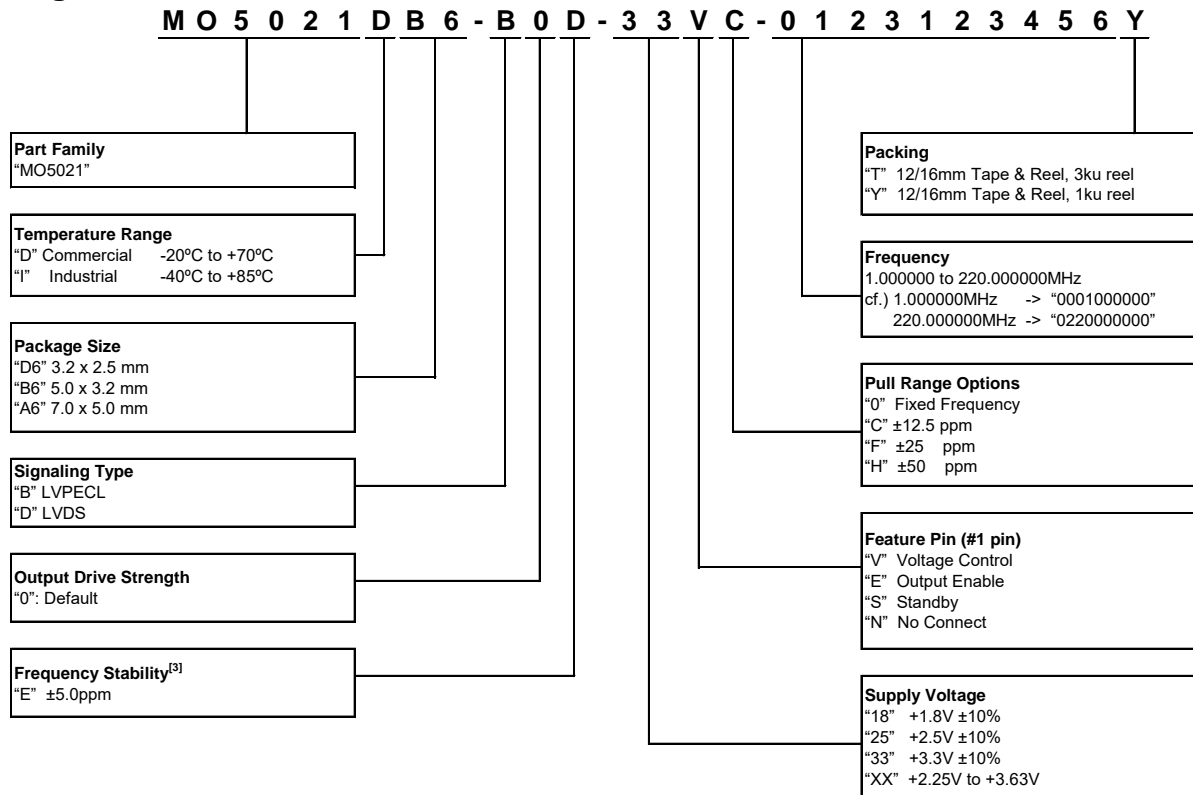
Dimensions and Patterns

Package Size – Dimensions (Unit: mm) ^[1]	Recommended Land Pattern (Unit: mm) ^[2]
<p>3.2 x 2.5x 0.75 mm</p>	
<p>5.0 x 3.2 x 0.75 mm</p>	
<p>7.0 x 5.0x 0.90 mm</p>	

Notes:

1. Top Marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
2. A capacitor of value 0.1 μ F between Vdd and GND is recommended.

Ordering Information



Note:

- Contact KDS for tighter stability options.

Ordering Codes for Supported Tape & Reel Packing Method

Device Size	12 mm T&R (3ku)	12 mm T&R (1ku)	12 mm T&R (250u)	16 mm T&R (3ku)	16 mm T&R (1ku)	16 mm T&R (250u)
7.0 x 5.0 mm	-	-	-	-	Y	X
5.0 x 3.2 mm	-	Y	X	-	-	-
3.2 x 2.5 mm	T	Y	X	-	-	-

Frequencies Not Supported

Range 1: From 209.000001 MHz to 210.999999 MHz

Revision History

Version	Release Date	Change Summary
1.2	8/20/13	Original
1.3	12/16/13	Added input specifications, LVPECL/LVDS waveforms, packaging T&R options
1.4	12/11/14	Modified Thermal Consideration values and Pin Configuration table (pin 1) and drawing
1.5	11/12/15	<ul style="list-style-type: none">• Revised stability over temperature and first year aging values in the electrical characteristics table• Revised frequency stability and supply voltage options