MO8208
Ultra-Performance Oscillator

KDS DAISHINKU CORP.

Features

- Any frequency between 1 and 80 MHz accurate to 6 decimal places
- 100% pin-to-pin drop-in replacement to quartz-based oscillators
- Ultra-low phase jitter: 0.5 ps (12 kHz to 20 MHz)
- Frequency stability as low as ±10 PPM
- Industrial or extended commercial temperature range
- LVCMOS/LVTTL compatible output
- Standard 4-pin packages: 2.7 x 2.4 (compatible with 2.5 x 2.0 footprint), 3.2 x 2.5, 5.0 x 3.2, 7.0 x 5.0 mm x mm
- Instant samples with Time Machine II and field programmable oscillators
- Outstanding silicon reliability of 2 FIT or 500 million hour MTBF
- Pb-free, RoHS and REACH compliant
- Ultra-short lead time

Applications

- SATA, SAS, Ethernet, PCI Express, video, WiFi
- Computing, storage, networking, telecom, industrial control

Pb-Free RoHS Compliant

Electrical Characteristics[1]

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Range						
Output Frequency Range	f	1	–	80	MHz	
Frequency Stability and Aging						
Frequency Stability	F_stab	-10	–	+10	PPM	Inclusive of Initial tolerance at +25 °C, and variations over operating temperature, rated power supply voltage and load
		-20	–	+20	PPM	
		-25	–	+25	PPM	
		-50	–	+50	PPM	
First year Aging	F_aging	-1.5	–	+1.5	PPM	+25°C
10-year Aging		-5.0	–	+5.0	PPM	+25°C
Operating Temperature Range						
Operating Temperature Range	T_use	-20	–	+70	°C	Extended Commercial
		-40	–	+85	°C	Industrial
Supply Voltage and Current Consumption						
Supply Voltage	Vdd	+1.71	+1.8	+1.89	V	Supply voltages between +2.5V and +3.3V can be supported. Contact KDS for additional information.
		+2.25	+2.5	+2.75	V	
		+2.52	+2.8	+3.08	V	
		+2.97	+3.3	+3.63	V	
Current Consumption	Idd	–	+31	+33	mA	No load condition, f = 20 MHz, Vdd = +2.5V, +2.8V or +3.3V
		–	+29	+31	mA	No load condition, f = 20 MHz, Vdd = +1.8V
OE Disable Current	I_OD	–	–	+31	mA	Vdd = +2.5V, +2.8V or +3.3V, OE = GND, output is Weakly Pulled Down
		–	–	+30	mA	Vdd = +1.8 V. OE = GND, output is Weakly Pulled Down
Standby Current	I_std	–	–	+70	µA	Vdd = +2.5V, +2.8V or +3.3V, $\overline{ST}$ = GND, output is Weakly Pulled Down
		–	–	+10	µA	Vdd = +1.8 V. $\overline{ST}$ = GND, output is Weakly Pulled Down
LVCMOS Output Characteristics						
Duty Cycle	DC	45	–	55	%	
Rise/Fall Time	Tr, Tf	–	1.2	2.0	ns	15 pF load, 10% - 90% Vdd
Output Voltage High	VOH	90%	–	–	Vdd	IOH = -6.0 mA, IOL = +6.0 mA, (Vdd = +3.3V, +2.8V, +2.5V) IOH = -3.0 mA, IOL = +3.0 mA, (Vdd = +1.8V)
Output Voltage Low	VOL	–	–	10%	Vdd	
Input Characteristics						
Input Voltage High	VIH	70%	–	–	Vdd	Pin 1, OE or $\overline{ST}$
Input Voltage Low	VIL	–	–	30%	Vdd	Pin 1, OE or $\overline{ST}$
Input Pull-up Impedance	Z_in	–	100	250	kΩ	Pin 1, OE logic high or logic low, or $\overline{ST}$ logic high
		2.0	–	–	MΩ	Pin 1, $\overline{ST}$ logic low

Note:
1. All electrical specifications in the above table are specified with 15 pF output load and for all Vdd(s) unless otherwise stated.

Electrical Characteristics[1] (Continued)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Startup and Resume Timing						
Startup Time	T_start	–	7.0	10	ms	Measured from the time Vdd reaches its rated minimum value
OE Enable/Disable Time	T_oe	–	–	150	ns	f = 80 MHz, For other frequencies, T_oe = 100 ns + 3 cycles
Resume Time	T_resume	–	6.0	10	ms	In standby mode, measured from the time $\overline{ST}$ pin crosses 50% threshold. Refer to Figure 5.
Jitter						
RMS Period Jitter	T_jitt	–	1.5	2.0	ps	
		–	2.0	3.0	ps	f = 75 MHz, Vdd = +1.8V
RMS Phase Jitter (random)	T_phj	–	0.5	1.0	ps	f = 10 MHz, Integration bandwidth = 12 kHz to 20 MHz

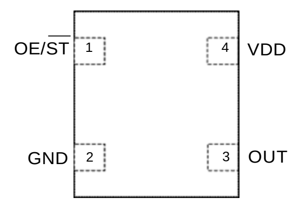
Note:

1. All electrical specifications in the above table are specified with 15 pF output load and for all Vdd(s) unless otherwise stated.

Pin Configuration

Pin	Symbol	Functionality	
1	OE/ $\overline{ST}$	Output Enable	H or Open[2]: specified frequency output L: output is high impedance. Only output driver is disabled.
		Standby	H or Open[2]: specified frequency output L: output is low (weak pull down). Device goes to sleep mode. Supply current reduces to I_std.
2	GND	Power	Electrical ground[3]
3	OUT	Output	Oscillator output
4	VDD	Power	Power supply voltage[3]

Top View



Notes:

2. A pull-up resistor of <10 kΩ between OE/ $\overline{ST}$ pin and Vdd is recommended in high noise environment.
3. A capacitor of value 0.1 µF between Vdd and GND is required.

Absolute Maximum

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	+150	°C
VDD	-0.5	+4.0	V
Electrostatic Discharge	–	+2000	V
Soldering Temperature (follow standard Pb free soldering guidelines)	–	+260	°C
Junction Temperature	–	+150	°C

Thermal Consideration

Package	θJA, 4 Layer Board (°C/W)	θJA, 2 Layer Board (°C/W)	θJC, Bottom (°C/W)
7050	191	263	30
5032	97	199	24
3225	109	212	27
2520	117	222	26

Environmental Compliance

Parameter	Condition/Test Method
Mechanical Shock	MIL-STD-883F, Method 2002
Mechanical Vibration	MIL-STD-883F, Method 2007
Temperature Cycle	JESD22, Method A104
Solderability	MIL-STD-883F, Method 2003
Moisture Sensitivity Level	MSL1 @ 260°C

Phase Noise Plot

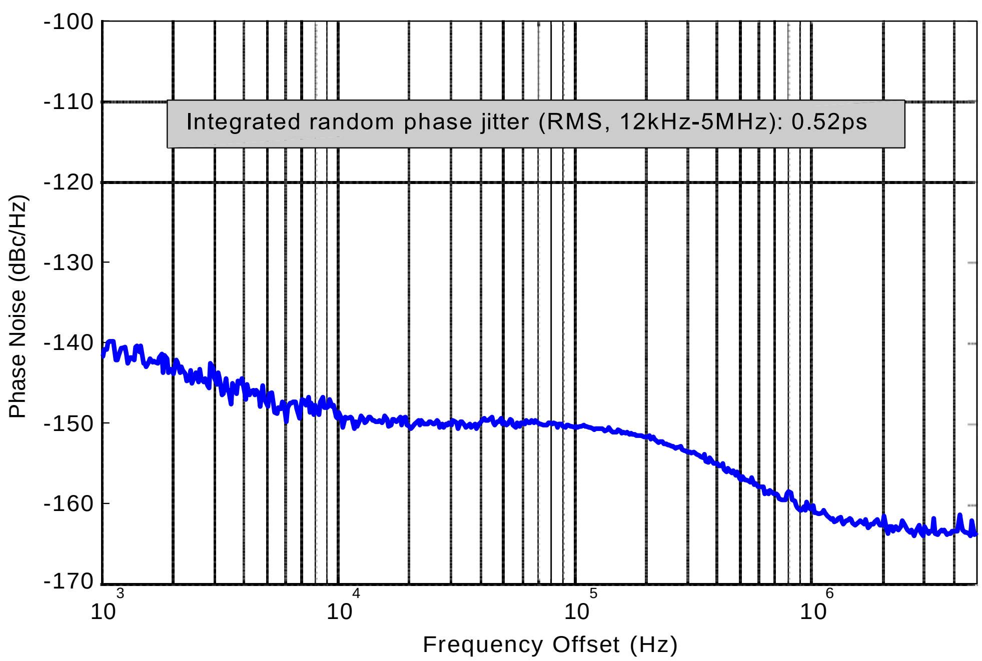


Figure 1. Phase Noise, 10 MHz, +3.3V, LVCMOS Output

Test Circuit and Waveform

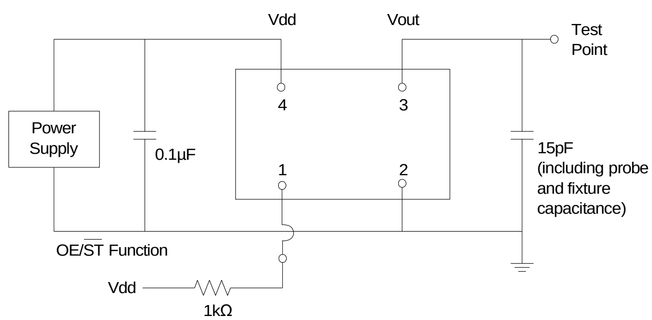


Figure 2. Test Circuit

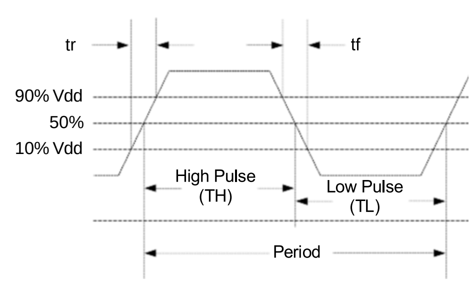
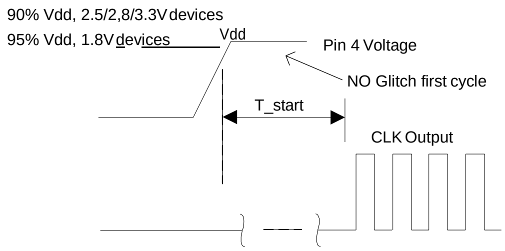


Figure 3. Waveform

Notes:

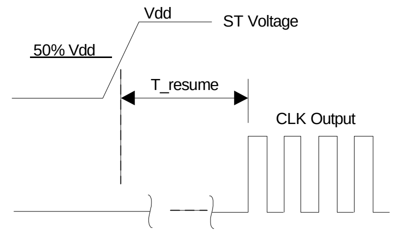
4. Duty Cycle is computed as Duty Cycle = TH/Period.
5. MO8208 supports the configurable duty cycle feature. For custom duty cycle at any given frequency, contact KDS.

Timing Diagram



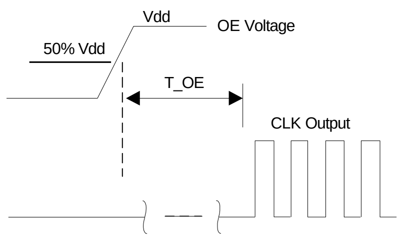
T_start: Time to start from power-off

Figure 4. Startup Timing (OE/$\overline{ST}$ Mode)



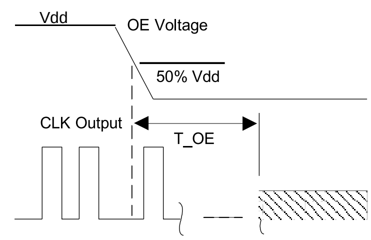
T_resume: Time to resume from ST

Figure 5. Standby Resume Timing ($\overline{ST}$ Mode Only)



T_OE: Time to re-enable the clock output

Figure 6. OE Enable Timing (OE Mode Only)



T_OE: Time to put the output drive in High Z mode

Figure 7. OE Disable Timing (OE Mode Only)

Notes:

6. MO8208 supports "no runt" pulses and "no glitch" output during startup or resume.
7. MO8208 supports gated output which is accurate within rated frequency stability from the first cycle.

Performance Plots[8]

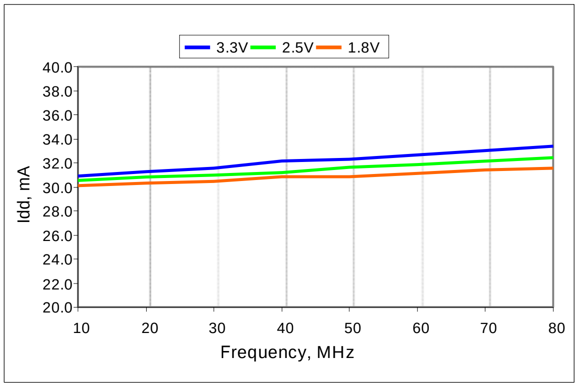


Figure 8. Idd vs Frequency

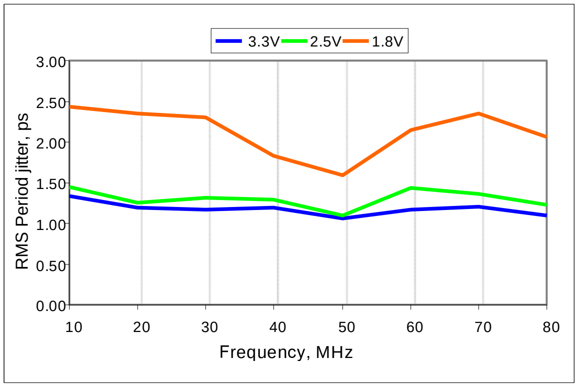


Figure 9. RMS Period Jitter vs Frequency

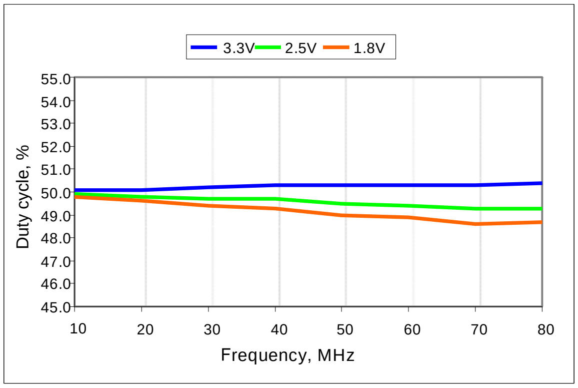


Figure 10. Duty Cycle vs Frequency

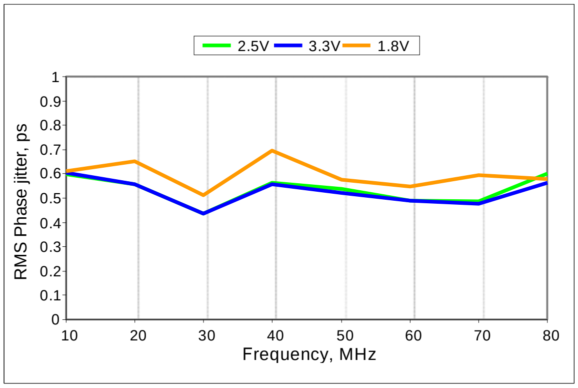


Figure 11. RMS Phase Jitter vs Frequency

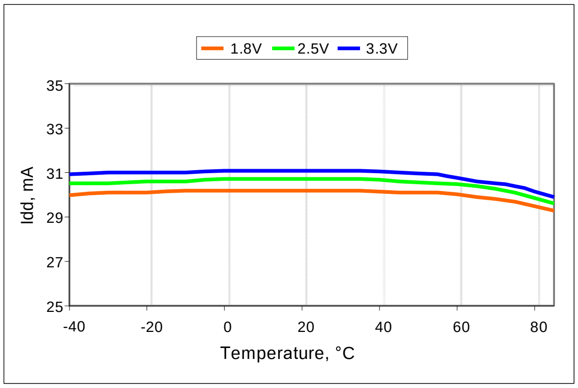


Figure 12. Idd vs Temperature, 10 MHz Output

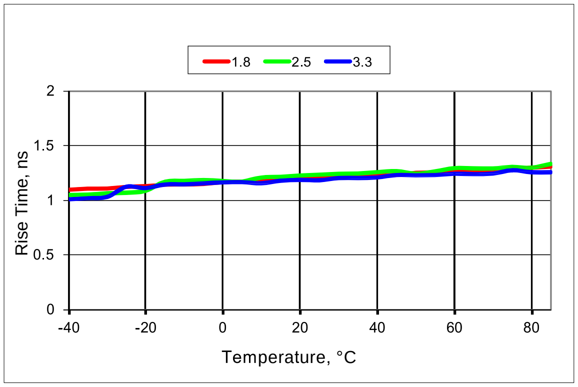


Figure 13. Rise Time vs Temperature, 75 MHz Output 10%-90% Vdd

Note:

8. All plots are measured with 15 pF load at room temperature, unless otherwise stated.

Programmable Drive Strength

The MO8208 includes a programmable drive strength feature to provide a simple, flexible tool to optimize the clock rise/fall time for specific applications. Benefits from the programmable drive strength feature are:

- Improves system radiated electromagnetic interference (EMI) by slowing down the clock rise/fall time
- Improves the downstream clock receiver's (RX) jitter by decreasing (speeding up) the clock rise/fall time.
- Ability to drive large capacitive loads while maintaining full swing with sharp edge rates.

For more detailed information about rise/fall time control and drive strength selection,

EMI Reduction by Slowing Rise/Fall Time

Figure 14 shows the harmonic power reduction as the rise/fall times are increased (slowed down). The rise/fall times are expressed as a ratio of the clock period. For the ratio of 0.05, the signal is very close to a square wave. For the ratio of 0.45, the rise/fall times are very close to near-triangular waveform. These results, for example, show that the 11th clock harmonic can be reduced by 35 dB if the rise/fall edge is increased from 5% of the period to 45% of the period.

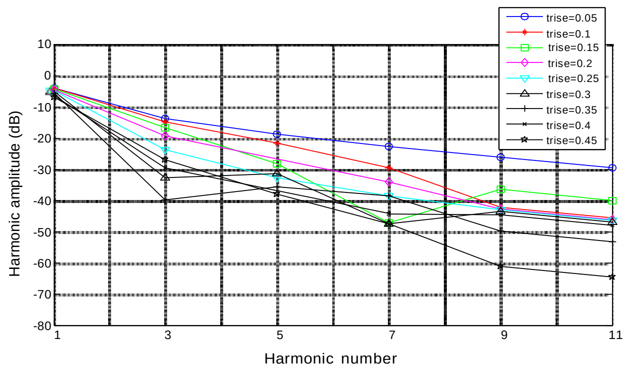


Figure 14. Harmonic EMI reduction as a Function of Slower Rise/Fall Time

Jitter Reduction with Faster Rise/Fall Time

Power supply noise can be a source of jitter for the downstream chipset. One way to reduce this jitter is to increase rise/fall time (edge rate) of the input clock. Some chipsets would require faster rise/fall time in order to reduce their sensitivity to this type of jitter. The MO8208 provides up to 3 additional high drive strength settings for very fast rise/fall time. Refer to the Rise/Fall Time Tables to determine the proper drive strength.

High Output Load Capability

The rise/fall time of the input clock varies as a function of the actual capacitive load the clock drives. At any given drive strength, the rise/fall time becomes slower as the output load increases. As an example, for a +3.3V MO8208 device with default drive strength setting, the typical rise/fall time is 1.15ns for 15 pF output load. The typical rise/fall time slows down to 2.72ns when the output load increases to 45 pF. One can choose to speed up the rise/fall time to 1.41ns by then increasing the drive strength setting on the MO8208.

The MO8208 can support up to 60 pF or higher in maximum capacitive loads with up to 3 additional drive strength settings. Refer to the Rise/Tall Time Tables to determine the proper drive strength for the desired combination of output load vs. rise/fall time

MO8208 Drive Strength Selection

Tables 1 through 5 define the rise/fall time for a given capacitive load and supply voltage.

1. Select the table that matches the MO8208 nominal supply voltage (+1.8V, +2.5V, +2.8V, +3.0V, +3.3V).
2. Select the capacitive load column that matches the application requirement (5 pF to 60 pF)
3. Under the capacitive load column, select the desired rise/fall times.
4. The left-most column represents the part number code for the corresponding drive strength.
5. Add the drive strength code to the part number for ordering purposes.

Calculating Maximum Frequency

Based on the rise and fall time data given in Tables 1 through 4, the maximum frequency the oscillator can operate with guaranteed full swing of the output voltage over temperature as follows:

$$\text{Max Frequency} = \frac{1}{3.5 \times Trf\_10/90}$$

Where Trf_10/90 is the typical rise/fall time at 10% to 90% Vdd.

Example 1

Calculate f_{MAX} for the following condition:

- Vdd = +1.8V (Table 1)
- Capacitive Load: 30 pF
- Typical Tr/f time = 5 ns (rise/fall time part number code =T)

Part number for the above example:

MO8208IF4-C**T**H-18E0-0057000000

Drive strength code is here.

Rise/Fall Time (10% to 90%) vs C_{LOAD} Tables

Table 1. Vdd = +1.8V Rise/Fall Times for Specific C_{LOAD}

Rise/Fall Time Typ (ns)					
Drive Strength \ C_{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF
L	12.45	17.68	19.48	46.21	57.82
A	6.50	10.27	16.21	23.92	30.73
R	4.38	7.05	11.61	16.17	20.83
B	3.27	5.30	8.89	12.18	15.75
S	2.62	4.25	7.20	9.81	12.65
D	2.19	3.52	6.00	8.31	10.59
T	1.76	3.01	5.14	7.10	9.15
E	1.59	2.59	4.49	6.25	7.98
U	1.49	2.28	3.96	5.55	7.15
F	1.22	2.10	3.57	5.00	6.46
W	1.07	1.88	3.23	4.50	5.87
G	1.01	1.64	2.95	4.12	5.40
X	0.96	1.50	2.74	3.80	4.98
K	0.92	1.41	2.56	3.52	4.64
Y	0.88	1.34	2.39	3.25	4.32
Q	0.86	1.29	2.24	3.04	4.06
Z or "0": Default	0.82	1.24	2.07	2.89	3.82
M	0.77	1.20	1.94	2.72	3.61
N	0.66	1.15	1.84	2.58	3.41
P	0.51	1.09	1.76	2.45	3.24

Table 2. Vdd = +2.5V Rise/Fall Times for Specific C_{LOAD}

Rise/Fall Time Typ (ns)					
Drive Strength \ C_{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF
L	8.68	13.59	18.36	32.70	42.06
A	4.42	7.18	11.93	16.60	21.38
R	2.93	4.78	8.15	11.19	14.59
B	2.21	3.57	6.19	8.55	11.04
S	1.67	2.87	4.94	6.85	8.80
D	1.50	2.33	4.11	5.68	7.33
T	1.06	2.04	3.50	4.84	6.26
E	0.98	1.69	3.03	4.20	5.51
U	0.93	1.48	2.69	3.73	4.92
F	0.90	1.37	2.44	3.34	4.42
W	0.87	1.29	2.21	3.04	4.02
G or "0": Default	0.67	1.20	2.00	2.79	3.69
X	0.44	1.10	1.86	2.56	3.43
K	0.38	0.99	1.76	2.37	3.18
Y	0.36	0.83	1.66	2.20	2.98
Q	0.34	0.71	1.58	2.07	2.80
Z	0.33	0.65	1.51	1.95	2.65
M	0.32	0.62	1.44	1.85	2.50
N	0.31	0.59	1.37	1.77	2.39
P	0.30	0.57	1.29	1.70	2.28

Table 3. Vdd = +2.8V Rise/Fall Times for Specific C_{LOAD}

Rise/Fall Time Typ (ns)					
Drive Strength \ C_{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF
L	7.93	12.69	17.94	30.10	38.89
A	4.06	6.66	11.04	15.31	19.80
R	2.68	4.40	7.53	10.29	13.37
B	2.00	3.25	5.66	7.84	10.11
S	1.59	2.57	4.54	6.27	8.07
D	1.19	2.14	3.76	5.21	6.72
T	1.00	1.79	3.20	4.43	5.77
E	0.94	1.51	2.78	3.84	5.06
U	0.90	1.38	2.48	3.40	4.50
F	0.87	1.29	2.21	3.03	4.05
W	0.62	1.19	1.99	2.76	3.68
G or "0": Default	0.41	1.08	1.84	2.52	3.36
X	0.37	0.96	1.72	2.33	3.15
K	0.35	0.78	1.63	2.15	2.92
Y	0.33	0.67	1.54	2.00	2.75
Q	0.32	0.63	1.46	1.89	2.57
Z	0.31	0.60	1.39	1.80	2.43
M	0.30	0.57	1.31	1.72	2.30
N	0.30	0.56	1.22	1.63	2.22
P	0.29	0.54	1.13	1.55	2.13

Table 4. Vdd = +3.3V Rise/Fall Times for Specific C_{LOAD}

Rise/Fall Time Typ (ns)					
Drive Strength \ C_{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF
L	7.18	11.59	17.24	27.57	35.57
A	3.61	6.02	10.19	13.98	18.10
R	2.31	3.95	6.88	9.42	12.24
B	1.65	2.92	5.12	7.10	9.17
S	1.43	2.26	4.09	5.66	7.34
D	1.01	1.91	3.38	4.69	6.14
T	0.94	1.51	2.86	3.97	5.25
E	0.90	1.36	2.50	3.46	4.58
U	0.86	1.25	2.21	3.03	4.07
F or "0": Default	0.48	1.15	1.95	2.72	3.65
W	0.38	1.04	1.77	2.47	3.31
G	0.36	0.87	1.66	2.23	3.03
X	0.34	0.70	1.56	2.04	2.80
K	0.33	0.63	1.48	1.89	2.61
Y	0.32	0.60	1.40	1.79	2.43
Q	0.32	0.58	1.31	1.69	2.28
Z	0.30	0.56	1.22	1.62	2.17
M	0.30	0.55	1.12	1.54	2.07
N	0.30	0.54	1.02	1.47	1.97
P	0.29	0.52	0.95	1.41	1.90

Instant Samples with Time Machine and Field Programmable Oscillators

KDS supports a field programmable version of the MO8208 low power oscillator for fast prototyping and real time customization of features. The field programmable devices (FP devices) are available for all five standard MO8208 package sizes and can be configured to one's exact specification using the Time Machine II, an USB powered MEMS oscillator programmer.

Customizable Features of the MO8208 FP Devices Include

- Any frequency between 1 – 80 MHz
- Three frequency stability options, ±20 PPM, ±25 PPM, ±50 PPM
- Two operating temperatures, -20 to +70°C or -40 to +85°C
- Five supply voltage options, +1.8V, +2.5V, +2.8V, +3.0V, and +3.3V
- Output drive strength

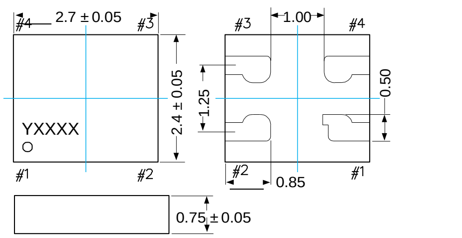
For more information regarding KDS's field programmable solutions, contact KDS.

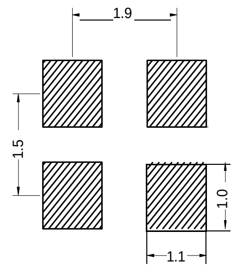
MO8208 is typically factory-programmed per customer ordering codes for volume delivery.

Dimensions and Patterns

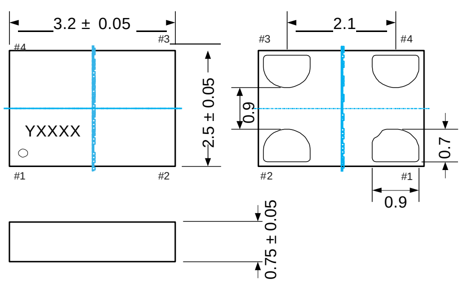
Package Size – Dimensions (Unit: mm) [9] | Recommended Land Pattern (Unit: mm) [10]

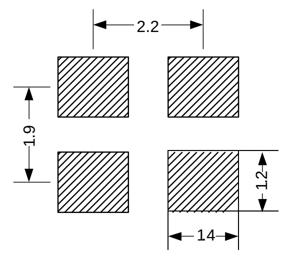
2.7 x 2.4 x 0.75 mm (100% compatible with 2.5 x 2. 0 mm footprint)



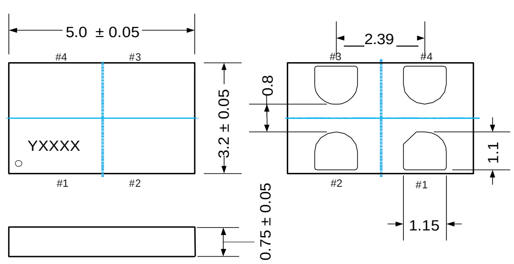


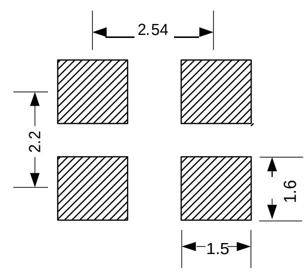
3.2 x 2.5 x 0.75 mm



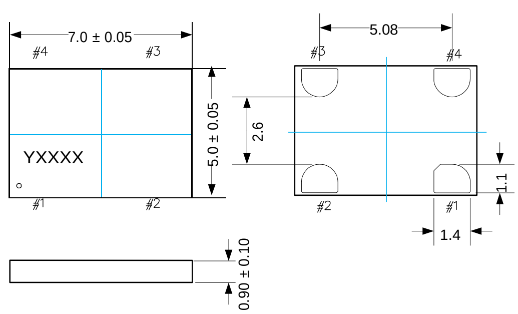


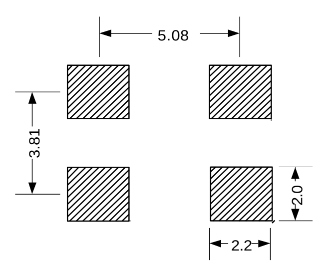
5.0 x 3.2 x 0.75 mm





7.0 x 5.0 x 0.90 mm





Notes:

9. Top marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of “Y” will depend on the assembly location of the device.
10. A capacitor of value 0.1 µF between Vdd and GND is required.

DAISHINKU CORP.

Ordering Information

M O 8 2 0 8 D D 4 - C 0 H - 2 5 E 0 - 0 0 7 5 1 2 3 4 5 6 Y

Part Family
"MO8208"

Temperature Range
"D" Ext. Commercial -20ºC to 70ºC
"I" Industrial -40ºC to 85ºC

Package Size
"F4" 2.7 x 2.4 mm
(compatible with 2.5 x 2.0 mm footprint)
"D4" 3.2 x 2.5 mm
"B4" 5.0 x 3.2 mm
"A4" 7.0 x 5.0 mm

Signaling Type
"C" LVCMOS

Output Drive Strength
See Table 1 to 5 for rise/fall times
"0": Default (datasheet limits)
"L" "S" "U" "X" "Z"
"A" "D" "F" "K" "M"
"R" "T" "W" "Y" "N"
"B" "E" "G" "Q" "P"

Frequency Stability
"F" ±10ppm
"G" ±20ppm
"H" ±25ppm
"K" ±50ppm

Packing
"Y" 12/16mm Tape & Reel, 1ku reel

Frequency
1.000000 to 80.000000MHz
cf.) 1.000000MHz -> "0001000000"
80.000000MHz -> "0080000000"

Function
"0" No Function

Feature Pin (#1 pin)
"E" Output Enable
"S" Standby

Supply Voltage
"18" +1.8V ±10%
"25" +2.5V ±10%
"28" +2.8V ±10%
"33" +3.3V ±10%