MO8209

High Frequency, Ultra Performance Oscillator



Features

- Any frequency between 80.000001 and 220 MHz accurate to 6 decimal places
- 100% pin-to-pin drop-in replacement to quartz-based oscillators
- Ultra-low phase jitter: 0.5 ps (12 kHz to 20 MHz)
- Frequency stability as low as ±10 PPM
- Industrial or extended commercial temperature range
- LVCMOS/LVTTL compatible output
- Standard 4-pin packages: 2.7 x 2.4 (compatible with 2.5 x 2.0 footprint), 3.2 x 2.5, 5.0 x 3.2, 7.0 x 5.0 mm x mm
- Outstanding silicon reliability of 2 FIT or 500 million hour MTBF
- Pb-free, RoHS and REACH compliant
- Ultra-short lead time

Applications

- SATA, SAS, Ethernet, 10-Gigabit Ethernet, SONET, PCI Express, video, Wireless
- Computing, storage, networking, telecom, industrial control





Electrical Characteristics

Parameter	Symbol	Min.	Тур.	Max.	Unit	Condition
Output Frequency Range	f	80.000001	-	220	MHz	
Frequency Stability		-10	ı	+10	PPM	
	F -4-b	-20	-	+20	PPM	Inclusive of Initial tolerance at +25 °C, and variations over
	F_stab	-25	-	+25	PPM	operating temperature, rated power supply voltage and load
		-50	ı	+50	PPM	
O	T	-20	-	+70	°C	Extended Commercial
Operating Temperature Range	T_use	-40	_	+85	°C	Industrial
		+1.71	+1.8	+1.89	V	
O and Walkers	Vdd	+2.25	+2.5	+2.75	V	Supply voltages between +2.5V and +3.3V can be supported.
Supply Voltage	vaa	+2.52	+2.8	+3.08	V	Contact KDS for guaranteed performance specs for supply voltages not specified in this table.
		+2.97	+3.3	+3.63	V	
Current Concumution	ldd	-	+34	+36	mA	No load condition, f = 100 MHz, Vdd = +2.5V, +2.8V or +3.3V
Current Consumption	luu	-	+30	+33	mA	No load condition, f = 100 MHz, Vdd = +1.8V
		-	ı	+31	mA	Vdd = +2.5V, +2.8V or +3.3V, OE = GND,
OE Disable Current	I_OD					output is Weakly Pulled Down
		-	-	+30	mA	Vdd = +1.8 V. OE = GND, output is Weakly Pulled Down
	l_std	_	_	+70	μΑ	Vdd = +2.5V, +2.8V or+ 3.3V, ST = GND,
Standby Current						output is Weakly Pulled Down
		_	-	+10	μA	Vdd = +1.8 V. ST = GND, output is Weakly Pulled Down
Duty Cycle	DC	45	-	55	%	f <= 165 MHz, all Vdds.
		40	ı	60	%	f > 165 MHz, all Vdds.
Rise/Fall Time	Tr, Tf	-	1.2	2.0	ns	15 pF load, 10% - 90% Vdd
Output Voltage High	VOH	90%	-	-	Vdd	IOH = -6.0 mA, IOL = +6.0 mA, (Vdd = +3.3V, +2.8V, +2.5V) IOH = -3.0 mA, IOL = +3.0 mA, (Vdd = +1.8V)
Output Voltage Low	VOL	-	-	10%	Vdd	
Input Voltage High	VIH	70%	-	-	Vdd	Pin 1, OE or $\overline{\text{ST}}$
Input Voltage Low	VIL	-	_	30%	Vdd	Pin 1, OE or ST
	_ .	-	100	250	kΩ	Pin 1, OE logic high or logic low, or ST logichigh
Input Pull-up Impedance	Z_in	2.0	-	-	ΜΩ	Pin 1, ST logic low
Startup Time	T_start	_	7.0	10	ms	Measured from the time Vdd reaches its rated minimum value
OE Enable/Disable Time	T_oe	-	-	115	ns	f = 80 MHz, For other frequencies, T_oe = 100 ns + 3 cycles
Resume Time	T_resume	-	-	10	ms	In standby mode, measured from the time ST pin crosses 50% threshold. Refer to Figure 5.
RMS Period Jitter	T ""	-	1.5	2.0	ps	f = 156.25 MHz, Vdd = +2.5V, +2.8V or +3.3V
	T_jitt	-	2.0	3.0	ps	f = 156.25 MHz, Vdd = +1.8V
RMS Phase Jitter (random)	T_phj	-	0.5	1.0	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz
First year Aging		-1.5	_	+1.5	PPM	+25°C
10-year Aging	F_aging	-5.0	_	+5.0	PPM	+25°C
Note:		1	1		ı	

1. All electrical specifications in the above table are specified with 15 pF output load and for all Vdd(s) unless otherwise stated.

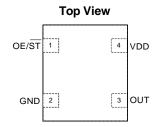
Daishinku Corp. 1389 Shinzaike, Hiraoka-cho, Kakogawa, Hyogo 675-0194 Japan

Revised June 25, 2013



Pin Configuration

Pin	Symbol		Functionality
		Output Enable	H or Open ^[2] : specified frequency output L: output is high impedance. Only output driver is disabled.
1	OE/ST	OE/ ST Standby	H or Open ^[2] : specified frequency output L: output is low (weak pull down). Device goes to sleep mode. Supply current reduces to I_std.
2	GND	Power	Electrical ground ^[3]
3	OUT	Output	Oscillator output
4	VDD	Power	Power supply voltage ^[3]



- 2. A pull-up resistor of <10 k Ω between OE/ $\overline{\text{ST}}$ pin and Vdd is recommended in high noise environment. 3. A capacitor of value 0.1 μF between Vdd and GND is recommended.

Absolute Maximum

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	+150	°C
VDD	-0.5	+4.0	V
Electrostatic Discharge	-	+2000	V
Soldering Temperature (follow standard Pb free soldering guidelines)	-	+260	°C
Junction Temperature	_	+150	°C

Thermal Consideration

Package	θJA, 4 Layer Board (°C/W)	θJA, 2 Layer Board (°C/W)	θJC, Bottom (°C/W)
7050	191	263	30
5032	97	199	24
3225	109	212	27
2520	117	222	26

Environmental Compliance

Parameter	Condition/Test Method
Mechanical Shock	MIL-STD-883F, Method2002
Mechanical Vibration	MIL-STD-883F, Method2007
Temperature Cycle	JESD22, Method A104
Solderability	MIL-STD-883F, Method2003
Moisture Sensitivity Level	MSL1 @ 260°C



Phase Noise Plot

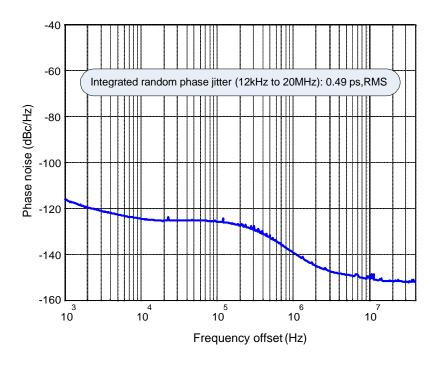


Figure 1. Phase Noise, 156.25 MHz, +3.3V, LVCMOS Output

Test Circuit and Waveform

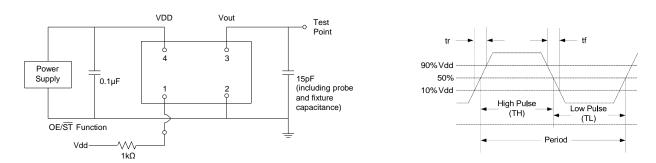


Figure 2. Test Circuit

Figure 3. Waveform

Notes:

- 4. Duty Cycle is computed as Duty Cycle = TH/Period.
- 5. MO8209 supports the configurable duty cycle feature. For custom duty at any given frequency, contact KDS.



Timing Diagram

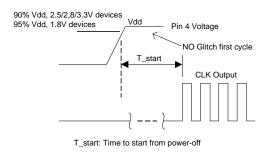


Figure 4. Startup Timing (OE/ST Mode)

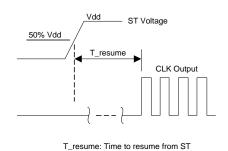


Figure 5. Standby Resume Timing (ST Mode Only)

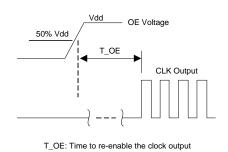
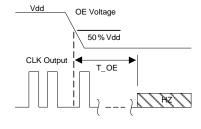


Figure 6. OE Enable Timing (OE Mode Only)



 $T_{\sf OE}\colon\quad {\sf Time} \ {\sf to} \ {\sf put} \ {\sf the} \ {\sf output} \ {\sf drive} \ {\sf in} \ {\sf High} \ {\sf Z} \ {\sf mode}$

Figure 7. OE Disable Timing (OE Mode Only)

- 6. MO8209 supports NO RUNT pulses and No glitches during startup or resume.7. MO8209 supports gated output which is accurate within rated frequency stability from the first cycle.



Performance Plots[8]

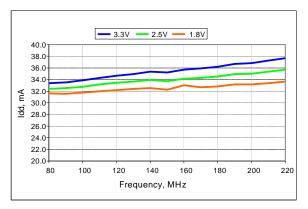


Figure 8. Idd vs Frequency

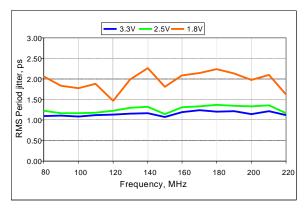


Figure 9. RMS Period Jitter vs Frequency

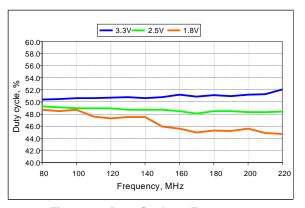


Figure 10. Duty Cycle vs Frequency

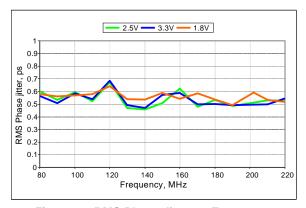


Figure 11. RMS Phase Jitter vs Frequency

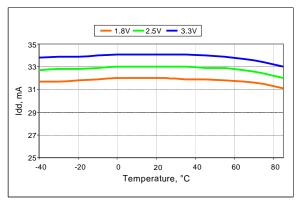


Figure 12. Idd vs Temperature, 100 MHz Output

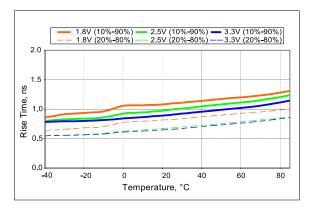


Figure 13. Rise Time vs Temperature, 100 MHz Output

Note:

8. All plots are measured with 15pF load at room temperature, unless otherwise stated.



Programmable Drive Strength

The MO8209 includes a programmable drive strength feature to provide a simple, flexible tool to optimize the clock rise/fall time for specific applications. Benefits from the programmable drive strength feature are:

- Improves system radiated electromagnetic interference (EMI) by slowing down the clock rise/fall time
- Improves the downstream clock receiver's (RX) jitter by decreasing (speeding up) the clock rise/fall time.
- Ability to drive large capacitive loads while maintaining full swing with sharp edge rates.

For more detailed information about rise/fall time control and drive strength selection, contact KDS.

EMI Reduction by Slowing Rise/Fall Time

Figure 14 shows the harmonic power reduction as the rise/fall times are increased (slowed down). The rise/fall times are expressed as a ratio of the clock period. For the ratio of 0.05, the signal is very close to a square wave. For the ratio of 0.45, the rise/fall times are very close to near-triangular waveform. These results, for example, show that the 11th clock harmonic can be reduced by 35 dB if the rise/fall edge is increased from 5% of the period to 45% of the period.

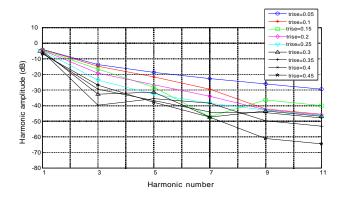


Figure 14. Harmonic EMI reduction as a Function of Slower Rise/Fall Time

Jitter Reduction with Faster Rise/Fall Time

Power supply noise can be a source of jitter for the downstream chipset. One way to reduce this jitter is to increase rise/fall time (edge rate) of the input clock. Some chipsets would require faster rise/fall time in order to reduce their sensitivity to this type of jitter. The MO8209 provides up to 3 additional high drive strength settings for very fast rise/fall time. Refer to the Rise/Fall Time Tables to determine the proper drive strength.

High Output Load Capability

The rise/fall time of the input clock varies as a function of the actual capacitive load the clock drives. At any given drive strength, the rise/fall time becomes slower as the output load increases. As an example, for a +3.3V MO8209 device with default drive strength setting, the typical rise/fall time is 1.15ns for 15 pF output load. The typical rise/fall time slows down to 2.72ns when the output load increases to 45 pF. One can

choose to speed up the rise/fall time to 1.41ns by then increasing the drive strength setting on the MO8209.

The MO8209 can support up to 60 pF or higher in maximum capacitive loads with up to 3 additional drive strength settings. Refer to the Rise/Tall Time Tables to determine the proper drive strength for the desired combination of output load vs. rise/fall time

MO8209 Drive Strength Selection

Tables 1 through 5 define the rise/fall time for a given capacitive load and supply voltage.

- 1. Select the table that matches the MO8209 nominal supply voltage (+1.8V, +2.5V, +2.8V, +3.0V, +3.3V).
- 2. Select the capacitive load column that matches the application requirement (5 pF to 60 pF)
- Under the capacitive load column, select the desired rise/fall times.
- 4. The left-most column represents the part number code for the corresponding drive strength.
- Add the drive strength code to the part number for ordering purposes.

Calculating Maximum Frequency

Based on the rise and fall time data given in Tables 1 through 4, the maximum frequency the oscillator can operate with guaranteed full swing of the output voltage over temperature as follows:

Max Frequency =
$$\frac{1}{6 \times (Trise)}$$

Example 1

Calculate f_{MAX} for the following condition:

- Vdd = +1.8V (Table 1)
- · Capacitive Load: 30 pF
- Desired Tr/f time = 3 ns (rise/fall time part number code = G)

Part number for the above example:

MO8209IF4-CGH-18E0-0055000000



Drive strength code is here.



Rise/Fall Time (10% to 90%) vs C_{LOAD} Tables

Table 1. Vdd = \pm 1.8V Rise/Fall Times for Specific C_{LOAD}

Table 2. Vdd = +2.5V Rise/Fall Times for Specific C_{LOAD}

Rise/Fall Time Typ (ns)							
Drive Strength \ C _{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF		
L	12.45	17.68	19.48	46.21	57.82		
Α	6.50	10.27	16.21	23.92	30.73		
R	4.38	7.05	11.61	16.17	20.83		
В	3.27	5.30	8.89	12.18	15.75		
S	2.62	4.25	7.20	9.81	12.65		
D	219	3.52	6.00	8.31	10.59		
T	1.76	3.01	5.14	7.10	9.15		
E	1.59	2.59	4.49	6.25	7.98		
U	1.49	2.28	3.96	5.55	7.15		
F	1.22	2.10	3.57	5.00	6.46		
W	1.07	1.88	3.23	4.50	5.87		
G	1.01	1.64	2.95	4.12	5.40		
X	0.96	1.50	2.74	3.80	4.98		
K	0.92	1.41	2.56	3.52	4.64		
Υ	0.88	1.34	2.39	3.25	4.32		
Q	0.86	1.29	2.24	3.04	4.06		
Z or "0": Default	0.82	1.24	2.07	2.89	3.82		
М	0.77	1.20	1.94	2.72	3.61		
N	0.66	1.15	1.84	2.58	3.41		
P	0.51	1.09	1.76	2.45	3.24		

Rise/Fall Time Typ (ns)						
Drive Strength \ C _{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF	
L	8.68	13.59	18.36	32.70	42.06	
Α	4.42	7.18	11.93	16.60	21.38	
R	2.93	4.78	8.15	11.19	14.59	
В	2.21	3.57	6.19	8.55	11.04	
S	1.67	2.87	4.94	6.85	8.80	
D	1.50	2.33	4.11	5.68	7.33	
Т	1.06	2.04	3.50	4.84	6.26	
E	0.98	1.69	3.03	4.20	5.51	
U	0.93	1.48	2.69	3.73	4.92	
F	0.90	1.37	2.44	3.34	4.42	
W	0.87	1.29	2.21	3.04	4.02	
G or "0": Default	0.67	1.20	2.00	2.79	3.69	
X	0.44	1.10	1.86	2.56	3.43	
K	0.38	0.99	1.76	2.37	3.18	
Υ	0.36	0.83	1.66	2.20	2.98	
Q	0.34	0.71	1.58	2.07	2.80	
Z	0.33	0.65	1.51	1.95	2.65	
M	0.32	0.62	1.44	1.85	2.50	
N	0.31	0.59	1.37	1.77	2.39	
Р	0.30	0.57	1.29	1.70	2.28	

Table 3. Vdd = +2.8V Rise/Fall Times for Specific C_{LOAD}

Table 4. Vdd = +3.3V Rise/Fall Times for Specific C_{LOAD}

Rise/Fall Time Typ (ns)						
Drive Strength \ C _{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF	
L	7.93	12.69	17.94	30.10	38.89	
Α	4.06	6.66	11.04	15.31	19.80	
R	2.68	4.40	7.53	10.29	13.37	
В	2.00	3.25	5.66	7.84	10.11	
S	1.59	2.57	4.54	6.27	8.07	
D	1.19	2.14	3.76	5.21	6.72	
T	1.00	1.79	3.20	4.43	5.77	
E	0.94	1.51	2.78	3.84	5.06	
U	0.90	1.38	2.48	3.40	4.50	
F	0.87	1.29	2.21	3.03	4.05	
W	0.62	1.19	1.99	2.76	3.68	
G or "0": Default	0.41	1.08	1.84	2.52	3.36	
Х	0.37	0.96	1.72	2.33	3.15	
K	0.35	0.78	1.63	2.15	2.92	
Υ	0.33	0.67	1.54	2.00	2.75	
Q	0.32	0.63	1.46	1.89	2.57	
Z	0.31	0.60	1.39	1.80	2.43	
M	0.30	0.57	1.31	1.72	2.30	
N	0.30	0.56	1.22	1.63	2.22	
Р	0.29	0.54	1.13	1.55	2.13	

Rise/Fall Time Typ (ns)							
Drive Strength \ C _{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF		
L	7.18	11.59	17.24	27.57	35.57		
A	3.61	6.02	10.19	13.98	18.10		
R	2.31	3.95	6.88	9.42	12.24		
В	1.65	2.92	5.12	7.10	9.17		
S	1.43	2.26	4.09	5.66	7.34		
D	1.01	1.91	3.38	4.69	6.14		
Т	0.94	1.51	2.86	3.97	5.25		
Е	0.90	1.36	2.50	3.46	4.58		
U	0.86	1.25	2.21	3.03	4.07		
F or "0": Default	0.48	1.15	1.95	2.72	3.65		
W	0.38	1.04	1.77	2.47	3.31		
G	0.36	0.87	1.66	2.23	3.03		
Х	0.34	0.70	1.56	2.04	2.80		
K	0.33	0.63	1.48	1.89	2.61		
Υ	0.32	0.60	1.40	1.79	2.43		
Q	0.32	0.58	1.31	1.69	2.28		
Z	0.30	0.56	1.22	1.62	2.17		
M	0.30	0.55	1.12	1.54	2.07		
N	0.30	0.54	1.02	1.47	1.97		
P	0.29	0.52	0.95	1.41	1.90		

MO8209

High Frequency, Ultra Performance Oscillator



Instant Samples with Time Machine and Field Programmable Oscillators

KDS supports a field programmable version of the MO8209 low power oscillator for fast prototyping and real time customization of features. The field programmable devices (FP devices) are available for all five standard MO8209 package sizes and can be configured to one's exact specification using the Time Machine II, an USB powered MEMS oscillator programmer.

Customizable Features of the MO8209 FP Devices Include

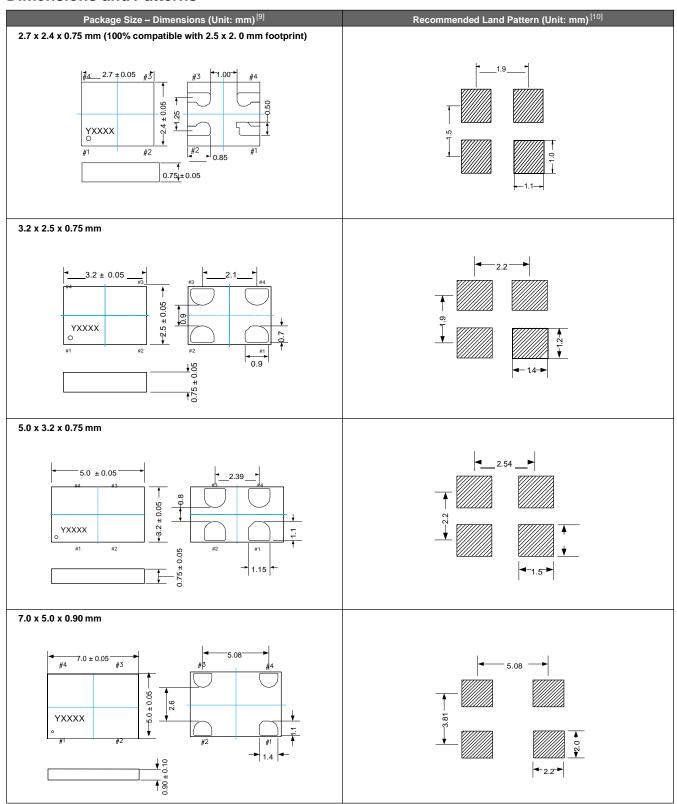
- Any frequency between 1 110 MHz
- Three frequency stability options, ±20 PPM, ±25 PPM, ±50 PPM
- Two operating temperatures, -20 to +70°C or -40 to +85°C
- Five supply voltage options, +1.8V, +2.5V, +2.8V, +3.0V, and +3.3V
- · Output drive strength

For more information regarding KDS's field programmable solutions, contact KDS.

MO8209 is typically factory-programmed per customer ordering codes for volume delivery.



Dimensions and Patterns



9. Top marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.

10. A capacitor of value 0.1 µF between Vdd and GND is recommended.



Ordering Information

