0.3 ps Jitter Oscillator for Networking



Features

- 25 MHz, 25.001200 MHz and 25.000625 MHz for Ethernet applications SATA, SAS, Ethernet, 10Gb Ethernet, XAUI
- 100% pin-to-pin drop-in replacement to quartz-based oscillators
- Ultra-low phase jitter: 0.3 ps
- Frequency stability as low as ±10 PPM
- Industrial or extended commercial temperature range
- LVCMOS/LVTTL compatible output
- Standby or output enable modes
- Standard 4-pin packages: 2.7 x 2.4 (compatible with 2.5 x 2.0 footprint), 3.2 x 2.5, 5.0 x 3.2, 7.0 x 5.0 mm x mm
- Outstanding silicon reliability of 2 FIT or 500 million hour MTBF
- Pb-free, RoHS and REACH compliant
- Ultra-short lead time

Applications

- Computing, storage, networking, telecom, industrial control





Electrical Characteristics^[1]

Parameter	Symbol	Min.	Тур.	Max.	Unit	Condition	
Output Frequency Range	f	25.000000,	25.001200,	25.000625	MHz		
Frequency Stability		-10	_	+10	PPM		
		-20	1	+20	PPM	Inclusive of Initial tolerance at +25 °C, and variations over	
	F_stab	-25	1	+25	PPM	operating temperature, rated power supply voltage and load	
		-50	_	+50	PPM		
On anti Town and - Bound	т	-20	ı	+70	°C	Extended Commercial	
Operating Temperature Range	T_use	-40	1	+85	°C	Industrial	
	Vdd	+1.71	+1.8	+1.89	V		
Supply Voltage		+2.25	+2.5	+2.75	V	Supply voltages between +2.5V and +3.3V can be supported. Contact KDS for additional information.	
Supply Vollage		+2.52	+2.8	+3.08	V		
		+2.97	+3.3	+3.63	V		
Current Consumption	ldd	-	+31	+33	mA	No load condition, f = 20 MHz, Vdd = +2.5V, +2.8V or +3.3V	
Current Consumption	idu	-	+29	+31	mA	No load condition, f = 20 MHz, Vdd = +1.8V	
OE Disable Current	I_OD	ı	ı	+31	mA	Vdd = +2.5V, +2.8V or +3.3V, OE = GND, output is Weakly Pulled Down	
		-	-	+30	mA	Vdd = +1.8 V. OE = GND, output is Weakly Pulled Down	
Standby Current	I_std	ı	ı	+70	μΑ	Vdd = +2.5V, +2.8V or +3.3V, \overline{ST} = GND, output is Weakly Pulled Down	
		1	1	+10	μΑ	Vdd = +1.8 V. ST = GND, output is Weakly Pulled Down	
Duty Cycle	DC	45	1	55	%		
Rise/Fall Time	Tr, Tf	-	1.2	2.0	ns	15 pF load, 10% - 90% Vdd	
Output Voltage High	VOH	90%	-	-	Vdd	IOH = -6.0 mA, IOL = +6.0 mA, (Vdd = +3.3V, +2.8V, +2.5V)	
Output Voltage Low	VOL	1	-	10%	Vdd	IOH = -3.0 mA, IOL = +3.0 mA, (Vdd = +1.8V)	
Input Voltage High	VIH	70%	-	-	Vdd	Pin 1, OE or ST	
Input Voltage Low	VIL	-	1	30%	Vdd	Pin 1, OE or ST	
	Z_in	-	100	250	kΩ	Pin 1, OE logic high or logic low, or ST logic high	
Input Pull-up Impedance		2.0	ı	-	ΜΩ	Pin 1, ST logic low	
Startup Time	T_start	_	7.0	10	ms	Measured from the time Vdd reaches its rated minimum value	
OE Enable/Disable Time	T_oe	-	-	150	ns		
Resume Time	T_resume	-	6.0	10	ms	In standby mode, measured from the time \overline{ST} pin crosses 50% threshold. Refer to Figure 5.	
RMS Period Jitter	T_jitt	-	1.5	2.0	ps	Vdd = +2.5V, +2.8V or +3.3V	
		-	2.0	3.0	ps	Vdd = +1.8V	
RMS Phase Jitter (random)	T_phj	_	0.25	0.3	ps	IEEE802.3-2005 10GbE jitter measurement specifications	
First year Aging		-1.5	_	+1.5	PPM	+25 °C	
10-year Aging	F_aging	-5.0	_	+5.0	PPM	+25 °C	
io year Aying		-5.0	_	+3.0	I I IVI	120 0	

Rev. 1.01

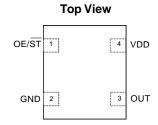
- 1. All electrical specifications in the above table are specified with 15 pF output load and for all Vdd(s) unless otherwise stated.
- 2. Contact KDS for custom drive strength to drive higher or multiple load, or SoftEdge™ option for EMI reduction.

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Pin Configuration

Pin	Symbol	Functionality		
1 OE/ ST	_	Output Enable	H or Open ^[3] : specified frequency output L: output is high impedance. Only output driver is disabled.	
	Standby	H or Open ^[3] : specified frequency output L: output is low (weak pull down). Device goes to sleep mode. Supply current reduces to I_std.		
2	GND	Power	Electrical ground	
3	OUT	Output	Oscillator output	
4	VDD	Power	Power supply voltage	



Notes:

3. A pull-up resistor of <10 k Ω between OE/ \overline{ST} pin and Vdd is recommended in high noise environment.

Absolute Maximum

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	+150	°C
VDD	-0.5	+4.0	V
Electrostatic Discharge	-	+2000	V
Soldering Temperature (follow standard Pb free soldering guidelines)	_	+260	°C

Thermal Consideration

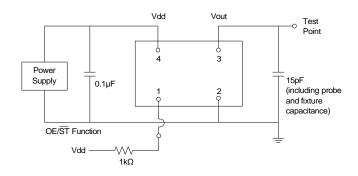
Package	θJA, 4 Layer Board (°C/W)	θJA, 2 Layer Board (°C/W)	θJC, Bottom (°C/W)
7050	191	263	30
5032	97	199	24
3225	109	212	27
2520	117	222	26

Environmental Compliance

Parameter	Condition/Test Method
Mechanical Shock	MIL-STD-883F, Method2002
Mechanical Vibration	MIL-STD-883F, Method 2007
Temperature Cycle	JESD22, Method A104
Solderability	MIL-STD-883F, Method 2003
Moisture Sensitivity Level	MSL1 @ 260°C



Test Circuit and Waveform



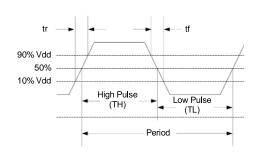


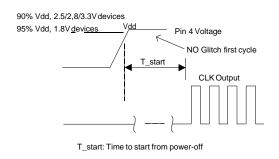
Figure 1. Test Circuit

Figure 2. Waveform

Notes:

- 4. Duty Cycle is computed as Duty Cycle = TH/Period.
- 5. MO8225 supports the configurable duty cycle feature. For custom duty cycle at any given frequency, contact KDS.

Timing Diagram



ST Voltage 50% Vdd T resume CLK Output

T_resume: Time to resume from ST

Figure 3. Startup Timing (OE/ST Mode)

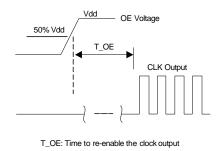
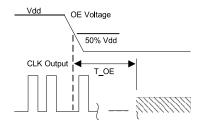


Figure 4. Standby Resume Timing (ST Mode Only)



T_OE: Time to put the output drive in High Z mode

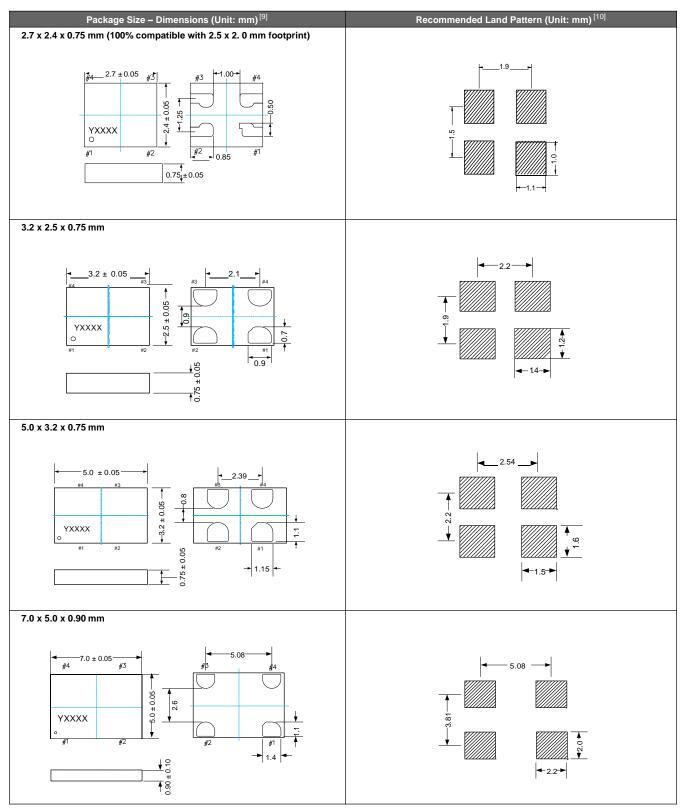
Figure 5. OE Enable Timing (OE Mode Only)

Figure 6. OE Disable Timing (OE Mode Only)

- 6. MO8225 supports "no runt" pulses and "no glitch" output during startup or resume.7. MO8225 supports gated output which is accurate within rated frequency stability from the first cycle.



Dimensions and Patterns

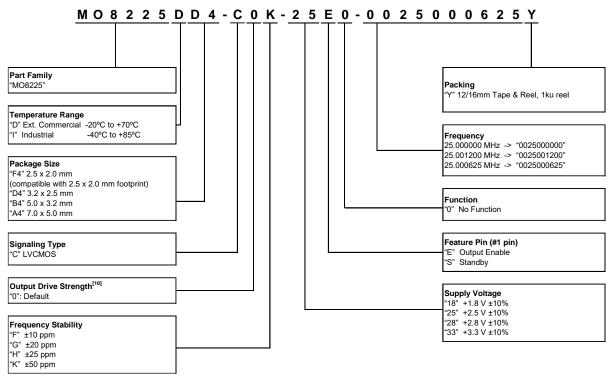


Notes

8. Top marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
9. A capacitor of value 0.1 µF between Vdd and GND is recommended.



Ordering Information



Notes:

10. Contact KDS for custom drive strength to drive higher or multiple load, or SoftEdge™ option for EMI reduction.