## Features

- Frequencies between 1 MHz and 110 MHz accurate to 6 decimal places
- Operating temperature from $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$
- Supply voltage of +1.8 V or +2.5 V to +3.3 V
- Excellent total frequency stability as low as $\pm 20 \mathrm{ppm}$
- Low power consumption of +3.5 mA typical at $20 \mathrm{MHz},+1.8 \mathrm{~V}$
- LVCMOS/LVTTL compatible output
- Industry-standard packages: $2.0 \times 1.6,2.5 \times 2.0,3.2 \times 2.5,5.0 \times 3.2$ $7.0 \times 5.0 \mathrm{~mm} \times \mathrm{mm}$
- Instant samples with Time Machine II and field programmable oscillators
- RoHS and REACH compliant, Pb-free, Halogen-free and Antimony-free


## Applications

- Ruggedized equipment in harsh operating environment


## Electrical Specifications

## Table 1. Electrical Characteristics

All Min and Max limits are specified over temperature and rated operating voltage with 15 pF output load unless otherwise stated. Typical values are at $+25^{\circ} \mathrm{C}$ and nominal supply voltage.

| Parameters | Symbol | Min. | Typ. | Max. | Unit | Condition |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Frequency Range |  |  |  |  |  |  |
| Output Frequency Range | f | 1 | - | 110 | MHz | Refer to Table 13 for the exact list of supported frequencies list of supported frequencies |
| Frequency Stability and Aging |  |  |  |  |  |  |
| Frequency Stability | F_stab | -20 | - | +20 | ppm | Inclusive of Initial tolerance at $+25^{\circ} \mathrm{C}$, 1 st year aging at $+25^{\circ} \mathrm{C}$, and variations over operating temperature, rated power supply voltage and load ( $15 \mathrm{pF} \pm 10 \%$ ). |
|  |  | -25 | - | +25 | ppm |  |
|  |  | -30 | - | +30 | ppm |  |
|  |  | -50 | - | +50 | ppm |  |
| Operating Temperature Range |  |  |  |  |  |  |
| Operating TemperatureRange | T_use | -55 | - | +125 | ${ }^{\circ} \mathrm{C}$ |  |
| Supply Voltage and Current Consumption |  |  |  |  |  |  |
| Supply Voltage | Vdd | +1.62 | +1.8 | +1.98 | V |  |
|  |  | +2.25 | +2.5 | +2.75 | V |  |
|  |  | +2.52 | +2.8 | +3.08 | V |  |
|  |  | +2.7 | +3.0 | +3.3 | V |  |
|  |  | +2.97 | +3.3 | +3.63 | V |  |
|  |  | +2.25 | - | +3.63 | V |  |
| Current Consumption | Idd | - | +3.8 | +4.7 | mA | No load condition, $\mathrm{f}=20 \mathrm{MHz}, \mathrm{Vdd}=+2.8 \mathrm{~V},+3.0 \mathrm{~V}$ or +3.3 V |
|  |  | - | +3.6 | +4.5 | mA | No load condition, $\mathrm{f}=20 \mathrm{MHz}, \mathrm{Vdd}=+2.5 \mathrm{~V}$ |
|  |  | - | +3.5 | +4.5 | mA | No load condition, $\mathrm{f}=20 \mathrm{MHz}, \mathrm{Vdd}=+1.8 \mathrm{~V}$ |
| OE Disable Current | I_od | - | - | +4.5 | mA | $\mathrm{Vdd}=+2.5 \mathrm{~V}$ to +3.3 V , $\mathrm{OE}=$ Low, Output in high Z state. |
|  |  | - | - | +4.3 | mA | $\mathrm{Vdd}=+1.8 \mathrm{~V}, \mathrm{OE}=$ Low, Output in high Zstate . |
| Standby Current | I_std | - | +2.6 | +8.5 | $\mu \mathrm{A}$ | $\mathrm{Vdd}=+2.8 \mathrm{~V}$ to $+3.3 \mathrm{~V}, \overline{\mathrm{ST}}=$ Low, Output is weakly pulled down |
|  |  | - | +1.4 | +5.5 | $\mu \mathrm{A}$ | $\mathrm{Vdd}=+2.5 \mathrm{~V}, \overline{\mathrm{ST}}=$ Low, Output is weakly pulled down |
|  |  | - | +0.6 | +4.0 | $\mu \mathrm{A}$ | $\mathrm{Vdd}=+1.8 \mathrm{~V}, \overline{\mathrm{ST}}=$ Low, Output is weakly pulled down |
| LVCMOS Output Characteristics |  |  |  |  |  |  |
| Duty Cycle | DC | 45 | - | 55 | \% | All Vdds |
| Rise/Fall Time | Tr, Tf | - | 1.0 | 2.0 | ns | $\mathrm{Vdd}=+2.5 \mathrm{~V},+2.8 \mathrm{~V},+3.0 \mathrm{~V}$ or $+3.3 \mathrm{~V}, 20 \%-80 \%$ |
|  |  | - | 1.3 | 2.5 | ns | $\mathrm{Vdd}=+1.8 \mathrm{~V}, 20 \%-80 \%$ |
|  |  | - | 1.0 | 3.0 | ns | $\mathrm{Vdd}=+2.25 \mathrm{~V}-3.63 \mathrm{~V}, 20 \%-80 \%$ |
| Output High Voltage | VOH | 90\% | - | - | Vdd | $\begin{aligned} & 1 \mathrm{OH}=-4.0 \mathrm{~mA}(\mathrm{Vdd}=+3.0 \mathrm{~V} \text { or }+3.3 \mathrm{~V}) \\ & 1 \mathrm{OH}=-3.0 \mathrm{~mA}(\mathrm{Vdd}=+2.8 \mathrm{~V} \text { or }+2.5 \mathrm{~V}) \\ & 1 \mathrm{OH}=-2.0 \mathrm{~mA}(\mathrm{Vdd}=+1.8 \mathrm{~V}) \end{aligned}$ |
| Output Low Voltage | VOL | - | - | 10\% | Vdd | $\begin{aligned} & \mathrm{IOL}=+4.0 \mathrm{~mA}(\mathrm{Vdd}=+3.0 \mathrm{~V} \text { or }+3.3 \mathrm{~V}) \\ & \mathrm{IOL}=+3.0 \mathrm{~mA}(\mathrm{Vdd}=+2.8 \mathrm{~V} \text { or }+2.5 \mathrm{~V}) \\ & \mathrm{IOL}=+2.0 \mathrm{~mA}(\mathrm{Vdd}=+1.8 \mathrm{~V}) \end{aligned}$ |

Table 1. Electrical Characteristics (continued)

| Parameters | Symbol | Min. | Typ. | Max. | Unit | Condition |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Input Characteristics |  |  |  |  |  |  |
| Input High Voltage | VIH | 70\% | - | - | Vdd | Pin 1, OE or $\overline{\text { ST }}$ |
| Input Low Voltage | VIL | - | - | 30\% | Vdd | Pin 1, OE or $\overline{\text { ST }}$ |
| Input Pull-up Impedence | Z_in | 50 | 87 | 150 | $\mathrm{k} \Omega$ | Pin 1, OE logic high or logic low, or $\overline{\mathrm{ST}}$ logic high |
|  |  | 2.0 | - | - | $\mathrm{M} \Omega$ | Pin 1, $\overline{\text { ST }}$ logic low |
| Startup and ResumeTiming |  |  |  |  |  |  |
| Startup Time | T_start | - | - | 5.0 | ms | Measured from the time Vdd reaches its rated minimum value |
| Enable/Disable Time | T_oe | - | - | 130 | ns | $\mathrm{f}=110 \mathrm{MHz}$. For other frequencies, T_oe = $100 \mathrm{~ns}+3$ * clock periods |
| Resume Time | T_resume | - | - | 5.0 | ms | Measured from the time $\overline{\mathrm{ST}}$ pin crosses $50 \%$ threshold |
| Jitter |  |  |  |  |  |  |
| RMS Period Jitter | T_jitt | - | 1.6 | 2.5 | ps | $\mathrm{f}=75 \mathrm{MHz}, \mathrm{Vdd}=+2.5 \mathrm{~V},+2.8 \mathrm{~V},+3.0 \mathrm{~V}$ or +3.3 V |
|  |  | - | 1.9 | 3.0 | ps | $\mathrm{f}=75 \mathrm{MHz}, \mathrm{Vdd}=+1.8 \mathrm{~V}$ |
| Peak-to-peak Period Jitter | T_pk | - | 12 | 20 | ps | $\mathrm{f}=75 \mathrm{MHz}, \mathrm{Vdd}=+2.5 \mathrm{~V},+2.8 \mathrm{~V},+3.0 \mathrm{~V}$ or +3.3 V |
|  |  | - | 14 | 25 | ps | $\mathrm{f}=75 \mathrm{MHz}, \mathrm{Vdd}=+1.8 \mathrm{~V}$ |
| RMS Phase Jitter (random) | T_phj | - | 0.5 | 0.8 | ps | $\mathrm{f}=75 \mathrm{MHz}$, Integration bandwidth $=900 \mathrm{kHz}$ to 7.5 MHz |
|  |  | - | 1.3 | 2.0 | ps | $\mathrm{f}=75 \mathrm{MHz}$, Integration bandwidth $=12 \mathrm{kHz}$ to 20 MHz |

Table 2. Pin Description

| Pin | Symbol |  | Functionality |
| :---: | :---: | :---: | :---: |
| 1 | $\mathrm{OE} / \overline{\mathrm{ST}} / \mathrm{NC}$ | Output Enable | $\mathrm{H}^{[1]}$ : specified frequency output <br> L : output is high impedance. Only output driver is disabled. |
|  |  | Standby | $\mathrm{H}^{[1]}$ : specified frequency output <br> L: output is low (weak pull down). Device goes to sleep mode. Supply current reduces to I_std. |
|  |  | No Connect | Any voltage between 0 and Vdd or Open ${ }^{[1]}$ : Specified frequency output. Pin 1 has no function. |
| 2 | GND | Power | Electrical ground |
| 3 | OUT | Output | Oscillator output |
| 4 | VDD | Power | Power supply voltage ${ }^{[2]}$ |



Figure 1. Pin Assignments

Notes:

1. In OE or $\overline{\text { ST }}$ mode, a pull-up resistor of 10kohm or less is recommended if pin 1 is not externally driven. If pin 1 needs to be left floating, use the NC option.
2. A capacitor of value $0.1 \mu \mathrm{~F}$ or higher between Vdd and GND is required.

Table 3. Absolute Maximum Limits
Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

| Parameter | Min. | Max. |  |
| :--- | :---: | :---: | :---: |
| Storage Temperature | -65 | +150 |  |
| Vdd | -0.5 | ${ }^{\circ} \mathrm{C}$ |  |
| Electrostatic Discharge | - | V |  |
| Soldering Temperature (follow standard Pb free soldering guidelines) | - | +2000 |  |
| Junction Temperature ${ }^{[3]}$ | - | +260 |  |

Note:
3. Exceeding this temperature for extended period of time may damage the device.

Table 4. Thermal Consideration ${ }^{[4]}$

| Package | OJA, 4 Layer Board <br> $\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$ | $\theta \mathrm{JA}, 2$ <br> $\left({ }^{( } \mathrm{C} / \mathrm{W}\right)$ | $\theta \mathrm{JC}$, Bottom <br> $\left({ }^{\circ} \mathrm{C} / W\right)$ |
| :---: | :---: | :---: | :---: |
| $\mathbf{7 0 5 0}$ | 142 | 273 | 30 |
| $\mathbf{5 0 3 2}$ | 97 | 199 | 24 |
| $\mathbf{3 2 5 5}$ | 109 | 212 | 27 |
| $\mathbf{2 5 2 0}$ | 117 | 222 | 26 |
| $\mathbf{2 0 1 6}$ | 152 | 252 | 36 |

Note:
4. Refer to JESD51-7 for $\theta$ JA and $\theta$ JC definitions, and reference layout used to determine the $\theta$ JA and $\theta$ JC values in the above table.

Table 5. Maximum Operating Junction Temperature ${ }^{[5]}$

| Max Operating Temperature(ambient) | Maximum Operating Junction Temperature |
| :---: | :---: |
| $+125^{\circ} \mathrm{C}$ | $+135^{\circ} \mathrm{C}$ |

Note:
5. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

Table 6. Environmental Compliance

| Parameter | Condition/Test Method |
| :--- | :--- |
| Mechanical Shock | MIL-STD-883F, Method2002 |
| Mechanical Vibration | MIL-STD-883F, Method2007 |
| Temperature Cycle | JESD22, Method A104 |
| Solderability | MIL-STD-883F, Method2003 |
| Moisture Sensitivity Level | MSL1 @ 260 ${ }^{\circ} \mathrm{C}$ |

## Test Circuit and Waveform ${ }^{[6]}$



Figure 2. Test Circuit
Note:
6. Duty Cycle is computed as Duty Cycle $=\mathrm{TH} /$ Period.

## Timing Diagrams



T_start: Time to start from power-off
Figure 4. Startup Timing ( $\mathrm{OE} / \overline{\mathrm{ST}}$ Mode)


T_oe: Time to re-enable the clock output
Figure 6. OE Enable Timing (OE Mode Only) Note:

[^0]

Figure 3. Waveform


Figure 5. Standby Resume Timing ( $\overline{\mathrm{ST}}$ Mode Only)


T_oe: Time to put the output in High Zmode
Figure 7. OE Disable Timing (OE Mode Only)

## Performance Plots ${ }^{[8]}$



Figure 8. Idd vs Frequency


Figure 10. RMS Period Jitter vs Frequency


Figure 12. 20\%-80\% Rise Time vs Temperature


Figure 9. Frequency vs Temperature


Figure 11. Duty Cycle vs Frequency


Figure 13. 20\%-80\% Fall Time vs Temperature

## Performance Plots ${ }^{[8]}$



Figure 14. RMS Integrated Phase Jitter Random (12k to 20 MHz ) vs Frequency ${ }^{[9]}$


Figure 15. RMS Integrated Phase Jitter Random ( 900 kHz to 20 MHz ) vs Frequency ${ }^{[9]}$

Notes:
8. All plots are measured with 15 pF load at room temperature, unless otherwise stated.
9. Phase noise plots are measured with Agilent E5052B signal source analyzer. Integration range is 12 kHz to 5 MHz for carrier frequencies up to 40 MHz .

## Programmable Drive Strength

The MO8920 includes a programmable drive strength feature to provide a simple, flexible tool to optimize the clock rise/fall time for specific applications. Benefits from the programmable drive strength feature are:

- Improves system radiated electromagnetic interference (EMI) by slowing down the clock rise/fall time
- Improves the downstream clock receiver's (RX) jitter by decreasing (speeding up) the clock rise/fall time.
- Ability to drive large capacitive loads while maintaining full swing with sharp edge rates.
For more detailed information about rise/fall time control and drive strength selection, contact KDS.


## EMI Reduction by Slowing Rise/Fall Time

Figure 16 shows the harmonic power reduction as the rise/fall times are increased (slowed down). The rise/fall times are expressed as a ratio of the clock period. For the ratio of 0.05 , the signal is very close to a square wave. For the ratio of 0.45 , the rise/fall times are very close to near-triangular waveform. These results, for example, show that the 11th clock harmonic can be reduced by 35 dB if the rise/fall edge is increased from $5 \%$ of the period to $45 \%$ of the period.


Figure 16. Harmonic EMI reduction as a Function of Slower Rise/Fall Time

## Jitter Reduction with Faster Rise/Fall Time

Power supply noise can be a source of jitter for the downstream chipset. One way to reduce this jitter is to speed up the rise/fall time of the input clock. Some chipsets may also require faster rise/fall time in order to reduce their sensitivity to this type of jitter. Refer to the Rise/Fall Time Tables (Table 7 to Table 11) to determine the proper drive strength.

## High Output Load Capability

The rise/fall time of the input clock varies as a function of the actual capacitive load the clock drives. At any given drive strength, the rise/fall time becomes slower as the output load increases. As an example, for a 3.3V MO8920 device with default drive strength setting, the typical rise/fall time is 1 ns for 15 pF output load. The typical rise/fall time slows down to 2.6 ns when the output load increases to 45 pF . One can choose to speed up the rise/fall time to 1.83 ns by then increasing the drive strength setting on the MO8920.

The MO8920 can support up to 60 pF or higher in maximum capacitive loads with drive strength settings. Refer to the Rise/Tall Time Tables (Table 7 to 11) to determine the proper drive strength for the desired combination of output load vs. rise/fall time

## MO8920 Drive Strength Selection

Tables 7 through 11 define the rise/fall time for a given capacitive load and supply voltage.

1. Select the table that matches the MO8920 nominal supply voltage ( $+1.8 \mathrm{~V},+2.5 \mathrm{~V},+2.8 \mathrm{~V},+3.0 \mathrm{~V},+3.3 \mathrm{~V}$ ).
2. Select the capacitive load column that matches the application requirement ( 5 pF to 60 pF )
3. Under the capacitive load column, select the desired rise/fall times.
4. The left-most column represents the part number code for the corresponding drive strength.
5. Add the drive strength code to the part number for ordering purposes.

## Calculating Maximum Frequency

Based on the rise and fall time data given in Tables 7 through 11, the maximum frequency the oscillator can operate with guaranteed full swing of the output voltage over temperature as follows:

$$
\text { Max Frequency }=\frac{1}{5 \times \text { Trf_20/80 }}
$$

where Trf_20/80 is the typical value for $20 \%-80 \%$ rise/fall time.

## Example 1

Calculate $\mathrm{f}_{\mathrm{MAX}}$ for the following condition:

- Vdd = +1.8V (Table 7)
- Capacitive Load: 30 pF
- Desired Tr/f time = 3 ns (rise/fall time part number code = E)

Part number for the above example:
MO8920MG4-CEH-18E0-0066666660


Drive strength code is here.

## Rise/Fall Time (20\% to 80\%) vs C LOAD Tables

Table 7. Vdd $=+1.8 \mathrm{~V}$ Rise/Fall Times for Specific $\mathrm{C}_{\text {LOAD }}$

| Rise/Fall Time Typ (ns) |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Drive Strength \C CoAD | $\mathbf{5} \mathbf{~ p F}$ | $\mathbf{1 5} \mathbf{p F}$ | $\mathbf{3 0} \mathbf{p F}$ | $\mathbf{4 5} \mathbf{p F}$ | $\mathbf{6 0} \mathbf{p F}$ |
| $\mathbf{L}$ | 6.16 | 11.61 | 22.00 | 31.27 | 39.91 |
| $\mathbf{A}$ | 3.19 | 6.35 | 11.00 | 16.01 | 21.52 |
| R | 2.11 | 4.31 | 7.65 | 10.77 | 14.47 |
| B | 1.65 | 3.23 | 5.79 | 8.18 | 11.08 |
| $\mathbf{T}$ | 0.93 | 1.91 | 3.32 | 4.66 | 6.48 |
| $\mathbf{E}$ | 0.78 | 1.66 | 2.94 | 4.09 | 5.74 |
| $\mathbf{U}$ | 0.70 | 1.48 | 2.64 | 3.68 | 5.09 |
| F or "0": default | 0.65 | 1.30 | 2.40 | 3.35 | 4.56 |

Table 9. Vdd $=+2.8 \mathrm{~V}$ Rise/Fall Times for Specific CLOAD

| Rise/Fall Time Typ (ns) |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Drive Strength \C CLOAD | $\mathbf{5} \mathbf{~ p F}$ | $\mathbf{1 5} \mathbf{~ p F}$ | $\mathbf{3 0} \mathbf{~ p F}$ | $\mathbf{4 5} \mathbf{~ p F}$ | $\mathbf{6 0} \mathbf{~ p F}$ |
| L | 3.77 | 7.54 | 12.28 | 19.57 | 25.27 |
| A | 1.94 | 3.90 | 7.03 | 10.24 | 13.34 |
| R | 1.29 | 2.57 | 4.72 | 7.01 | 9.06 |
| B | 0.97 | 2.00 | 3.54 | 5.43 | 6.93 |
| T | 0.55 | 1.12 | 2.08 | 3.22 | 4.08 |
| E or "0": default | 0.44 | 1.00 | 1.83 | 2.82 | 3.67 |
| U | 0.34 | 0.88 | 1.64 | 2.52 | 3.30 |
| F | 0.29 | 0.81 | 1.48 | 2.29 | 2.99 |

Table 8. Vdd = +2.5V Rise/Fall Times for Specific C LOAD

| Rise/Fall Time Typ (ns) |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Drive Strength \C CoAD | $\mathbf{5} \mathbf{p F}$ | $\mathbf{1 5} \mathbf{p F}$ | $\mathbf{3 0} \mathbf{p F}$ | $\mathbf{4 5} \mathbf{p F}$ | $\mathbf{6 0} \mathbf{p F}$ |
| $\mathbf{L}$ | 4.13 | 8.25 | 12.82 | 21.45 | 27.79 |
| A | 2.11 | 4.27 | 7.64 | 11.20 | 14.49 |
| R | 1.45 | 2.81 | 5.16 | 7.65 | 9.88 |
| B | 1.09 | 2.20 | 3.88 | 5.86 | 7.57 |
| $\mathbf{T}$ | 0.62 | 1.28 | 2.27 | 3.51 | 4.45 |
| E or "0": default | 0.54 | 1.00 | 2.01 | 3.10 | 4.01 |
| U | 0.43 | 0.96 | 1.81 | 2.79 | 3.65 |
| F | 0.34 | 0.88 | 1.64 | 2.54 | 3.32 |

Table 10. Vdd $=+3.0 \mathrm{~V}$ Rise/Fall Times for Specific CLOAD

| Rise/Fall Time Typ (ns) |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Drive Strength \C COAD | $\mathbf{5} \mathbf{~ p F}$ | $\mathbf{1 5} \mathbf{p F}$ | $\mathbf{3 0} \mathbf{p F}$ | $\mathbf{4 5} \mathbf{~ p F}$ | $\mathbf{6 0} \mathbf{~ p F}$ |
| $\mathbf{L}$ | 3.60 | 7.21 | 11.97 | 18.74 | 24.30 |
| $\mathbf{A}$ | 1.84 | 3.71 | 6.72 | 9.86 | 12.68 |
| R | 1.22 | 2.46 | 4.54 | 6.76 | 8.62 |
| B | 0.89 | 1.92 | 3.39 | 5.20 | 6.64 |
| T or "0": default | 0.51 | 1.00 | 1.97 | 3.07 | 3.90 |
| E | 0.38 | 0.92 | 1.72 | 2.71 | 3.51 |
| $\mathbf{U}$ | 0.30 | 0.83 | 1.55 | 2.40 | 3.13 |
| F | 0.27 | 0.76 | 1.39 | 2.16 | 2.85 |

Table 11. Vdd $=+3.3 \mathrm{~V}$ Rise/Fall Times for Specific $\mathrm{C}_{\text {LOAD }}$

| Rise/Fall Time Typ (ns) |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Drive Strength \Cload | 5 pF | 15 pF | 30 pF | 45 pF | 60 pF |
| L | 3.39 | 6.88 | 11.63 | 17.56 | 23.59 |
| A | 1.74 | 3.50 | 6.38 | 8.98 | 12.19 |
| R | 1.16 | 2.33 | 4.29 | 6.04 | 8.34 |
| B | 0.81 | 1.82 | 3.22 | 4.52 | 6.33 |
| T or "0": default | 0.46 | 1.00 | 1.86 | 2.60 | 3.84 |
| E | 0.33 | 0.87 | 1.64 | 2.30 | 3.35 |
| U | 0.28 | 0.79 | 1.46 | 2.05 | 2.93 |
| F | 0.25 | 0.72 | 1.31 | 1.83 | 2.61 |

## Pin 1 Configuration Options (OE, $\overline{\mathrm{ST}}$, or NC)

Pin 1 of the MO8920 can be factory-programmed to support three modes: Output enable (OE), standby ( $\overline{\mathrm{ST}}$ ) or No Connect (NC). These modes can also be programmed with the Time Machine using field programmable devices.

## Output Enable (OE) Mode

In the OE mode, applying logic Low to the OE pin only disables the output driver and puts it in $\mathrm{Hi}-\mathrm{Z}$ mode. The core of the device continues to operate normally. Power consumption is reduced due to the inactivity of the output. When the OE pin is pulled High, the output is typically enabled in $<1 \mu \mathrm{~s}$.

## Standby ( $\overline{\mathbf{S T}}$ ) Mode

In the ST mode, a device enters into the standby mode when Pin 1 pulled Low. All internal circuits of the device are turned off. The current is reduced to a standby current, typically in the range of a few $\mu \mathrm{A}$. When $\overline{\mathrm{ST}}$ is pulled High, the device goes through the "resume" process, which can take up to 5 ms .

## No Connect (NC) Mode

In the NC mode, the device always operates in its normal mode and output the specified frequency regardless of the logic level on pin 1.
Table 12 below summarizes the key relevant parameters in the operation of the device in $\mathrm{OE}, \overline{\mathrm{ST}}$, or NC mode.
Table 12. OE vs. $\overline{\text { ST }}$ vs. NC

|  | OE | $\overline{\mathrm{ST}}$ | NC |
| :--- | :---: | :---: | :---: |
| Active current $20 \mathrm{MHz}(\max ,+1.8 \mathrm{~V})$ | +4.5 mA | +4.5 mA | +4.5 mA |
| OE disable current (max. +1.8 V ) | +4.3 mA | $\mathrm{~N} / \mathrm{A}$ | $\mathrm{N} / \mathrm{A}$ |
| Standby current (typical +1.8 V ) | $\mathrm{N} / \mathrm{A}$ | $+0.6 \mu \mathrm{~A}$ | $\mathrm{~N} / \mathrm{A}$ |
| OE enable time at $110 \mathrm{MHz}(\max )$ | 130 ns | $\mathrm{~N} / \mathrm{A}$ | $\mathrm{N} / \mathrm{A}$ |
| Resume time from standby <br> (max, all frequency) | $\mathrm{N} / \mathrm{A}$ | 5 ms | $\mathrm{~N} / \mathrm{A}$ |
| Output driver in OE disable/standby mode | High Z | weak <br> pull-down | $\mathrm{N} / \mathrm{A}$ |

## Output on Startup and Resume

The MO8920 comes with gated output. Its clock output is accurate to the rated frequency stability within the first pulse from initial device startup or resume from the standby mode.

In addition, the MO8920 has NO RUNT, NO GLITCH output during startup or resume as shown in the waveform captures in Figure 17 and Figure 18.


Figure 17. Startup Waveform vs. Vdd


Figure 18. Startup Waveform vs. Vdd (Zoomed-in View of Figure 17)

## Instant Samples with Time Machine and Field Programmable Oscillators

KDS supports a field programmable version of the MO8920 high temperature oscillator for fast prototyping and real time customization of features. The field programmable devices (FP devices) are available for all five standard MO8920 package sizes and can be configured to one's exact specification using the Time Machine II, an USB powered MEMS oscillator programmer.

## Customizable Features of the MO8920 FP Devices Include

- Frequencies between $1-110 \mathrm{MHz}$
- Four frequency stability options, $\pm 20 \mathrm{ppm}, \pm 25 \mathrm{ppm}$, $\pm 30 \mathrm{ppm}, \pm 50 \mathrm{ppm}$
- Six supply voltage options, $+1.8 \mathrm{~V},+2.5 \mathrm{~V},+2.8 \mathrm{~V},+3.0 \mathrm{~V},+3.3 \mathrm{~V}$ and +2.25 to +3.63 V continuous
- Output drive strength

For more information regarding KDS's field programmable solutions, contact KDS.

MO8920 is factory-programmed per customer ordering codes for volume delivery.

## Dimensions and Patterns

$2.0 \times 1.6 \times 0.75 \mathrm{~mm}$

## Dimensions and Patterns



Notes:
10. Top marking: $Y$ denotes manufacturing origin and $X X X X$ denotes manufacturing lot number. The value of " $Y$ " will depend on the assembly location of the device. 11. A capacitor of value $0.1 \mu \mathrm{~F}$ or higher between Vdd and GND is required.

## Ordering Information



| Frequency Stability |
| :--- |
| "G" $\pm 20 \mathrm{ppm}$ |
| "H" $\pm 25 \mathrm{ppm}$ |
| "J" $\pm 30 \mathrm{ppm}$ |
| "K" $\pm 50 \mathrm{ppm}$ |

Frequency
Refer to the Supported Frequency Table below

Function
"0" No Function

```
Feature Pin (#1 pin)
"E" Output Enable
"S" Standby
"N" No Connect
```

Table 13. List of Supported Frequencies ${ }^{[12,13]}$

| Frequency Range <br> $\left(-55\right.$ to $\left.+125^{\circ} \mathrm{C}\right)$ |  |
| :---: | :---: |
| Min. | Max. |
| 1.000000 MHz | 61.222999 MHz |
| 61.674001 MHz | 69.239999 MHz |
| 70.827001 MHz | 78.714999 MHz |
| 79.561001 MHz | 80.159999 MHz |
| 80.174001 MHz | 80.779999 MHz |
| 82.632001 MHz | 91.833999 MHz |
| 95.474001 MHz | 96.191999 MHz |
| 96.209001 MHz | 96.935999 MHz |
| 99.158001 MHz | 110.000000 MHz |

Notes:
12. Any frequency within the min and max values in the above table are supported with 6 decimal places of accuracy.
13. Please contact KDS for frequencies that are not listed in the tables above.

Table 14. Ordering Codes for Supported Tape \& Reel Packing Method

| Device Size (mm x mm) | 16 mm T\&R (3ku) | 16 mm T\&R (1ku) | $12 \mathrm{~mm} \mathrm{~T} \mathrm{\& R} \mathrm{(3ku)}$ | $12 \mathrm{~mm} \mathrm{~T} \mathrm{\& R}$ (1ku) | 8 mm T\&R (3ku) | $8 \mathrm{~mm} \mathrm{~T} \mathrm{\& R} \mathrm{(1ku)}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $2.0 \times 1.6$ | - | - | - | - | D | E |
| $2.5 \times 2.0$ | - | - | - | - | D | E |
| $3.2 \times 2.5$ | - | - | - | - | D | E |
| $5.0 \times 3.2$ | - | - | - | Y | - | - |
| $7.0 \times 5.0$ | - | Y | - | - | - | - |

## Revision History

Table 15. Datasheet Version and Change Log

| Version | Release Date |  |
| :---: | :---: | :--- |
| 1.0 | $5 / 7 / 15$ | Final production release |
| 1.01 | $6 / 18 / 15$ | - Added 16 mm T\&R information to Table 14 |
|  |  | Revised 12 mm T\&R information to Table 14 |


[^0]:    7. MO8920 has "no runt" pulses and "no glitch" output during startup or resume.
