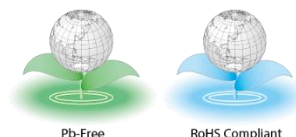


Features

- 0.3 ps RMS phase jitter (random) for 10GbE applications
- Frequency stability as low as ± 10 ppm
- 100% drop-in replacement for quartz and SAW oscillators
- Configurable positive frequency shift, +25, +50, or +75 ppm
- Industry-standard packages: 3.2 x 2.5, 5.0 x 3.2, 7.0 x 5.0 mmxmm
- Best in class 1-year and 10-year aging
- Best resilience, up to 40x better than quartz
- For other frequencies, refer to SiT9121 or 9122 datasheet

Applications

- 10GB Ethernet, SONET, SATA, SAS, Fibre Channel, PCI-Express
- Telecom, networking, instrumentation, storage, servers



Electrical Characteristics

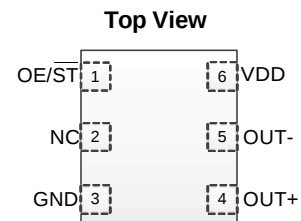
Parameter and Conditions	Symbol	Min.	Typ.	Max.	Unit	Condition
LVPECL and LVDS, Common Electrical Characteristics						
Supply Voltage	V _{dd}	+2.97	+3.3	+3.63	V	
		+2.25	+2.5	+2.75	V	
		+2.25	—	+3.63	V	Termination schemes in Figures 1 and 2 - XX ordering code
Output Frequency Range	f	156.25000, 156.253906, 156.257812, 156.261718, 161.132800			MHz	156.253906 MHz, +25 PPM from 156.250000 156.257812 MHz, +50 PPM from 156.250000 156.261718 MHz, +75 PPM from 156.250000
Frequency Stability	F _{stab}	-10	—	+10	ppm	Inclusive of initial tolerance, operating temperature, rated power supply voltage, and load variations
		-20	—	+20	ppm	
		-25	—	+25	ppm	
		-50	—	+50	ppm	
First Year Aging	F _{aging1}	-2.0	—	+2.0	ppm	+25°C
10-year Aging	F _{aging10}	-5.0	—	+5.0	ppm	+25°C
Operating Temperature Range	T _{use}	-40	—	+85	°C	Industrial
		-20	—	+70	°C	Extended Commercial
Input Voltage High	V _{IH}	70%	—	—	V _{dd}	Pin 1, OE or $\overline{ST}$
Input Voltage Low	V _{IL}	—	—	30%	V _{dd}	Pin 1, OE or $\overline{ST}$
Input Pull-up Impedance	Z _{in}	—	100	250	k Ω	Pin 1, OE logic high or logic low, or $\overline{ST}$ logic high
		2.0	—	—	M Ω	Pin 1, $\overline{ST}$ logic low
Start-up Time	T _{start}	—	6.0	10	ms	Measured from the time V _{dd} reaches its rated minimum value.
Resume Time	T _{resume}	—	6.0	10	ms	In Standby mode, measured from the time $\overline{ST}$ pin crosses 50% threshold.
Duty Cycle	DC	45	—	55	%	Contact KDS for tighter duty cycle
LVPECL, DC and AC Characteristics						
Current Consumption	I _{dd}	—	+61	+69	mA	Excluding Load Termination Current, V _{dd} = +3.3V or +2.5V
OE Disable Supply Current	I _{OE}	—	—	+35	mA	OE = Low
Output Disable Leakage Current	I _{leak}	—	—	+1.0	μ A	OE = Low
Standby Current	I _{std}	—	—	+100	μ A	$\overline{ST}$ = Low, for all V _{dds}
Maximum Output Current	I _{driver}	—	—	+30	mA	Maximum average current drawn from OUT+ or OUT-
Output High Voltage	V _{OH}	V _{dd} -1.1	—	V _{dd} -0.7	V	See Figure 1(a)
Output Low Voltage	V _{OL}	V _{dd} -1.9	—	V _{dd} -1.5	V	See Figure 1(a)
Output Differential Voltage Swing	V _{Swing}	+1.2	+1.6	+2.0	V	See Figure 1(b)
Rise/Fall Time	T _r , T _f	—	300	500	ps	20% to 80%, see Figure 1(a)
OE Enable/Disable Time	T _{oe}	—	—	120	ns	f = 156.25 MHz - For other frequencies, T _{oe} = 100ns + 3 period
RMS Phase Jitter (random)	T _{phj}	—	0.25	0.3	ps	IEEE802.3-2005 10GbE jitter measurement specifications
LVDS, DC and AC Characteristics						
Current Consumption	I _{dd}	—	+47	+55	mA	Excluding Load Termination Current, V _{dd} = +3.3V or +2.5V
OE Disable Supply Current	I _{OE}	—	—	+35	mA	OE = Low
Differential Output Voltage	V _{OD}	+250	+350	+450	mV	See Figure 2

Electrical Characteristics (continued)

Parameter and Conditions	Symbol	Min.	Typ.	Max.	Unit	Condition
LVDS, DC and AC Characteristics (continued)						
Output Disable Leakage Current	I_{leak}	–	–	+1.0	μA	OE = Low
Standby Current	I_{std}	–	–	+100	μA	$\overline{ST}$ = Low, for all Vdds
VOD Magnitude Change	ΔVOD	–	–	+50	mV	See Figure 2
Offset Voltage	VOS	+1.125	+1.2	+1.375	V	See Figure 2
VOS Magnitude Change	ΔVOS	–	–	+50	mV	See Figure 2
Rise/Fall Time	T_r, T_f	–	495	600	ps	20% to 80%, see Figure 2
OE Enable/Disable Time	T_{oe}	–	–	115	ns	$f = 156.25$ MHz - For other frequencies, $T_{oe} = 100ns + 3$ period
RMS Phase Jitter (random)	T_{phj}	–	0.25	0.3	ps	IEEE802.3-2005 10GbE jitter measurement specifications

Pin Description

Pin	Map		Functionality
1	OE	Input	H or Open: specified frequency output L: output is high impedance
	$\overline{ST}$	Input	H or Open: specified frequency output L: Device goes to sleep mode. Supply current reduces to I_{std} .
2	NC	NA	No Connect; Leave it floating or connect to GND for better heat dissipation
3	GND	Power	VDD Power Supply Ground
4	OUT+	Output	Oscillator output
5	OUT-	Output	Complementary oscillator output
6	VDD	Power	Power supply voltage



Absolute Maximum

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	+150	$^{\circ}C$
VDD	-0.5	+4.0	V
Electrostatic Discharge (HBM)	–	+2000	V
Soldering Temperature (follow standard Pb free soldering guidelines)	–	+260	$^{\circ}C$

Thermal Consideration

Package	θ_{JA} , 4 Layer Board ($^{\circ}C/W$)	θ_{JC} , Bottom ($^{\circ}C/W$)
7050, 6-pin	142	27
5032, 6-pin	97	20
3225, 6-pin	109	20

Environmental Compliance

Parameter	Condition/Test Method
Mechanical Shock	MIL-STD-883F, Method2002
Mechanical Vibration	MIL-STD-883F, Method2007
Temperature Cycle	JESD22, Method A104
Solderability	MIL-STD-883F, Method2003
Moisture Sensitivity Level	MSL1 @ 260 $^{\circ}C$

Waveform Diagrams

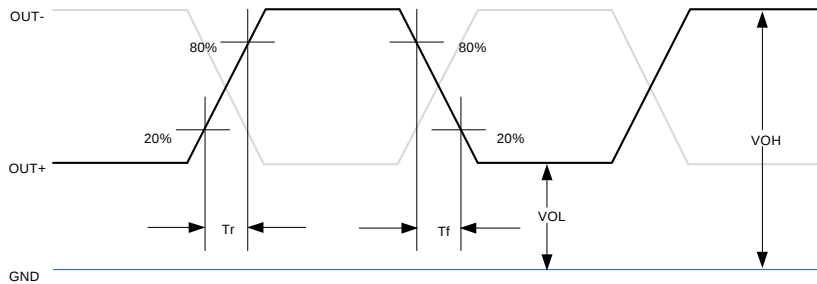


Figure 1(a). LVPECL Voltage Levels per Differential Pin (OUT+/OUT-)

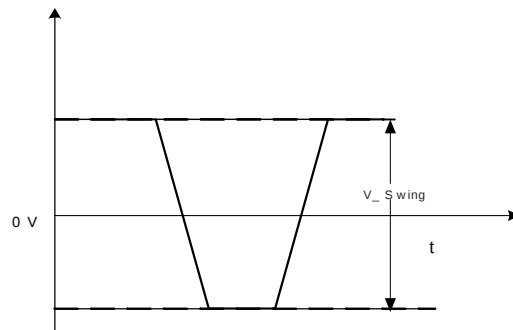


Figure 1(b). LVPECL Voltage Levels Across Differential Pair

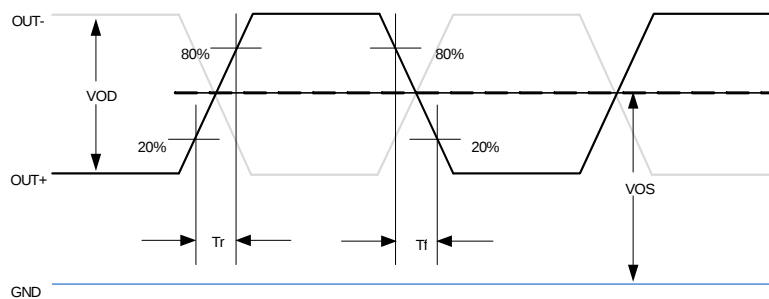


Figure 2. LVDS Voltage Levels per Differential Pin (OUT+/OUT-)

Termination Diagrams

LVPECL:

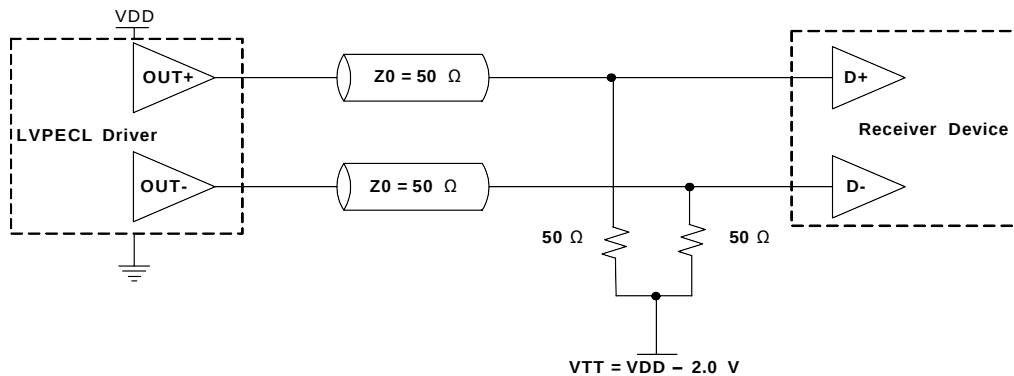


Figure 3. LVPECL Typical Termination

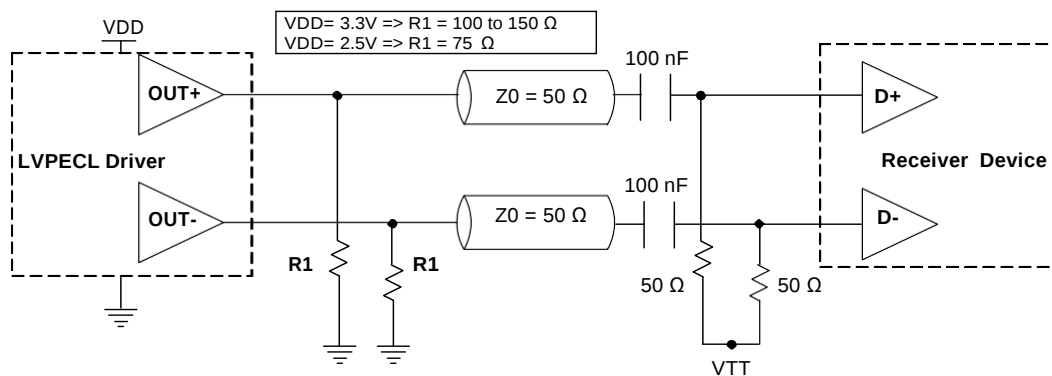


Figure 4. LVPECL AC Coupled Termination

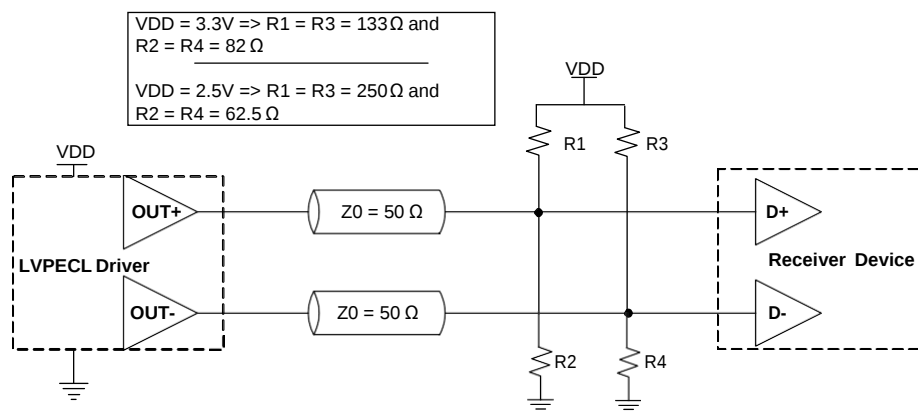


Figure 5. LVPECL with Thevenin Typical Termination

LVDS:

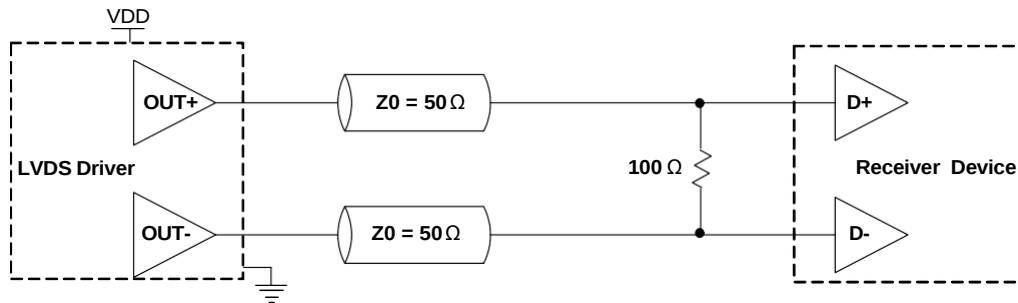
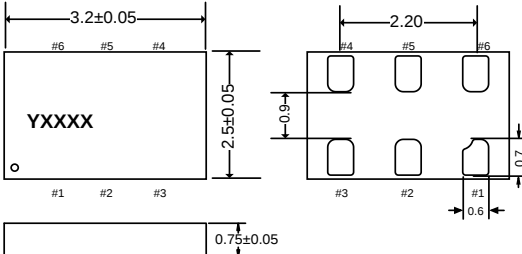
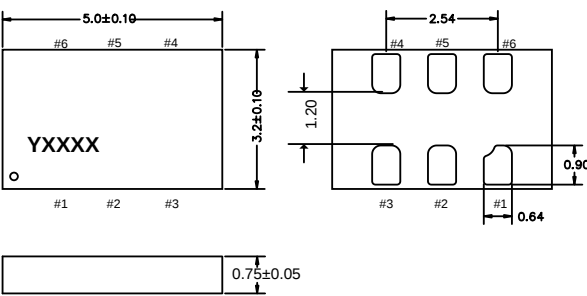
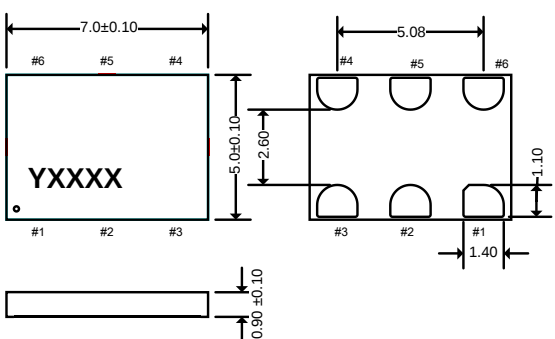


Figure 6. LVDS Single Termination (Load Terminated)

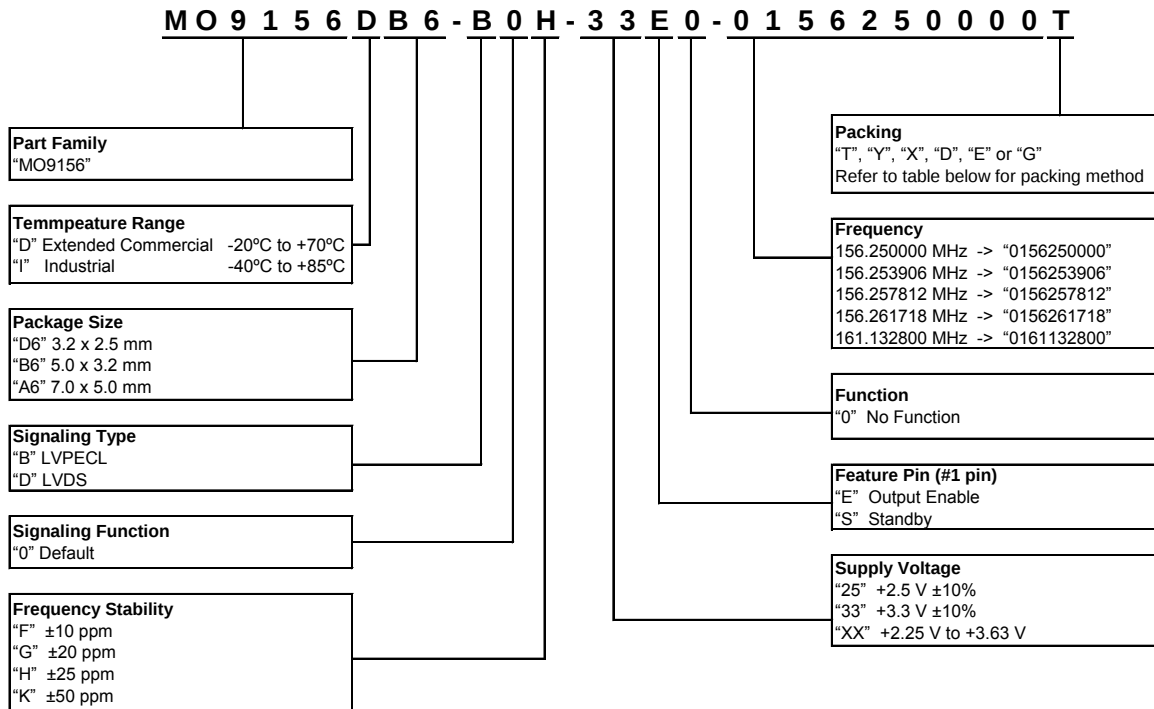
Dimensions and Patterns

Package Size – Dimensions (Unit: mm) ^[1]	Recommended Land Pattern (Unit: mm) ^[2]
3.2 x 2.5 x 0.75 mm 	
5.0 x 3.2 x 0.75 mm 	
7.0 x 5.0 x 0.90 mm 	

Notes:

1. Top Marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
2. A capacitor of value 0.1 μ F between Vdd and GND is recommended.

Ordering Information



Ordering Codes for Supported Tape & Reel Packing Method

Device Size	8 mm T&R (3ku)	8 mm T&R (1ku)	8 mm T&R (250u)	12 mm T&R (3ku)	12 mm T&R (1ku)	12 mm T&R (250u)	16 mm T&R (3ku)	16 mm T&R (1ku)	16 mm T&R (250u)
7.0 x 5.0 mm	-	-	-	-	-	-	T	Y	X
5.0 x 3.2 mm	-	-	-	T	Y	X	-	-	-
3.2 x 2.5 mm	D	E	G	-	-	-	-	-	-

Revision History

Version	Release Date	Change Summary
1.01	2/20/13	Original
1.02	12/3/13	Added input specifications, LVPECL/LVDS waveforms, packaging T&R options
1.03	2/6/14	Added 8mm T&R option
1.04	3/3/14	Added ± 10 ppm
1.05	7/23/14	Include Thermal Consideration Table
1.06	10/6/14	Modified Thermal Consideration values