

## **MEMS Oscillators - Low Jitter**

# MO9120/MO9121/MO9122/MO8208/MO8209



### ■Features

- Frequency tolerance as low as ±10×10<sup>-6</sup>
  Ultra-Low phase Jitter

- ApplicationsComputing, storage, networkingTelecom, industrial control
- SATA, SAS, Ethernet, PCI Express, video, WiFi





**RoHS Compliant** 

Model	Output Frequency (MHz)	Frequency Tolerance (×10 <sup>-6</sup> )	Supply Voltage (V)	Current Consumption (mA Typ.)	Size (mm)	Output
MO9120	25 to 212.5		+2.25 to +3.63	+54 to +69	3.2×2.5×0.8,	LVDECL
MO9121	1 to 220				$5.0 \times 3.2 \times 0.8$ ,	LVPECL LVDS
MO9122	220 to 625	±10, ±20, ±25, ±50			7.0×5.0×1.0 (QFN)	
MO8208	1 to 80			+29 to +36 (+10 μA stby)	2.7×2.4×0.8, 3.2×2.5×0.8,	LVCMOS
MO8209	80 to 220				5.0×3.2×0.8, 7.0×5.0×1.0 (QFN)	

### ■ Standard Specification (MO9121)

Item	Legend	Min.	Тур.	Max.	Unit	Condition	
Output Frequency Range	f	1	-	220	MHz	Refer to datasheet for exact list of supported frequencies	
		+2.97	+3.3	+3.63			
Supply Voltage	Vdd	+2.25	+2.5	+2.75	V		
		+2.25	-	+3.63			
Operating Temperature	т	-20	-	+70	$^{\circ}$	Extended Commercial	
Range	T_use	-40	-	+85		Industrial	
		-10	-	+10			
	F_stab	-20	_	+20	×10 <sup>-6</sup>	Inclusive of initial tolerance, and variations over operating temperature, rated power supply voltage and output load	
Frequency Tolerance		-25	_	+25			
		-50	_	+50			
First Year Aging	F_aging1	-2.0	_	+2.0		$T_A = +25^{\circ}C$	
10-year Aging	F_aging10	-5.0	_	+5.0	×10 <sup>-6</sup>	T <sub>^</sub> = +25℃	
Outy Cycle	DC	45	_	55	%	- A	
Input Low Voltage	V <sub>II</sub>	-	_	Vdd×0.3	V	Pin 1, OE or ST	
Input High Voltage	V <sub>IH</sub>	Vdd×0.7	_	_	V	Pin 1, OE or ST	
Start-up Time	T start	-	6.0	10	ms	Measured from the time Vdd reaches its rated minimum value	
•	_					In Standby mode, measured from the time ST pin crosses 50%	
Resume Time	T_resume	-	6.0	10	ms	threshold.	
			LVPECI	, DC and A	C Charac		
Current Consumption	ldd	_	+61	+69	mΑ	Excluding Load Termination Current, $Vdd = +3.3V$ or $+2.5V$	
OE Disable Supply Current	I_oe	-	-	+35	mA	OE = Low	
Standby Current	I_std	_	-	+100	μΑ	ST = Low, for all Vdds	
Output Low Voltage	V <sub>OL</sub>	Vdd - 1.9	_	Vdd - 1.5	V		
Output High Voltage	V <sub>OH</sub>	Vdd - 1.1	-	Vdd - 0.7	V		
Rise and Fall Time	Tr, Tf	-	300	700	ps	20% to 80%	
Enable and Disable Time	T_oe	-	_	115	ns	f = 212.5 MHz - For other frequencies, T_oe = 100ns + 3 period	
		_	1.2	1.7		f = 100 MHz, Vdd = +3.3V or +2.5V	
RMS Period Jitter	T_jitt		1.2	1.7	ps	f = 156.25 MHz, Vdd = +3.3V or +2.5V	
RIVIS Period Jitter			1.2	1.7		f = 212.5 MHz, Vdd = +3.3V or +2.5V	
DAAC Disease Piller (considere)							
RMS Phase Jitter (random)	T_phj	_	0.6	0.85	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdds	
		1		DC and AC		*	
Current Consumption	Idd	_	+47	+55	mA	Excluding Load Termination Current, Vdd = +3.3V or +2.5V	
OE Disable Supply Current	I_oe	-	_	+35	mA	OE = Low	
Standby Current	I_std	-		+100	μΑ	ST = Low, for all Vdds	
Rise and Fall Time	Tr,Tf	-	495	700	ps	20% to 80%	
Differential Output Voltage	V <sub>od</sub>	+250	+350	+450	mV		
V <sub>OD</sub> Magnitude Change	∠V <sub>OD</sub>	-	-	+50	mV		
Offset Voltage	Vos	+1.125	+1.2	+1.375	V		
V <sub>os</sub> Magnitude Change	∠Vos	_	-	+50	mV		
Enable and Disable Time	T_oe	_	-	115	ns	f = 212.5 MHz - For other frequencies, T_oe = 100ns + 3 period	
	T_jitt	-	1.2	1.7	ps	f = 100 MHz, Vdd = +3.3V or +2.5V	
RMS Period Jitter		_	1.2	1.7		f = 156.25 MHz, Vdd = +3.3V or +2.5V	
	-	_	1.2	1.7	•	f = 212.5 MHz, Vdd = +3.3V or +2.5V	
RMS Phase Jitter (random)	T_phj	_	0.6	0.85	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdds	
Packing Unit	-1- J		1000n			000pcs./reel (φ180: 3225 package)	