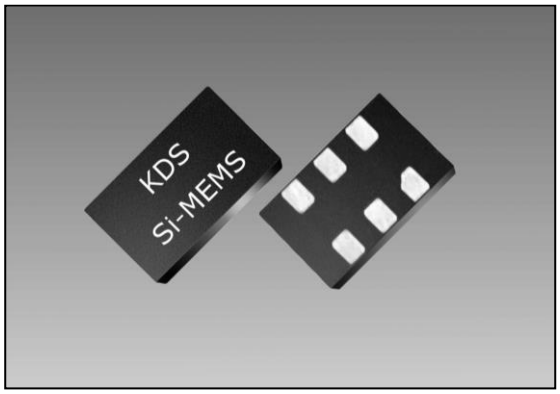
Low Phase Jitter MEMS Oscillator

KDS DAISHINKU CORP.

MO9156



■Features

- ●156.25000, 156.253906, 156.257812, 156.261718, 161.132800 MHz
- ●Industry-Standard packages: 3.2 x 2.5, 5.0 x 3.2 and 7.0 x 5.0 mm
- ●LVPECL and LVDS output signaling types
- ●Frequency stability as low as ±10 x 10^{-6}
- ●0.3 ps RMS phase jitter (random) for 10GbE applications
- ●For any other frequencies, refer to MO9121or MO9122 datasheet

■Applications

- ●10GB Ethernet, XAUI, SONET, SATA, Fibre Channel, PCI-Express
- ●Telecom, networking, instrumentation, storage, servers

Pb-Free RoHS Compliant

■Standard Specification

Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Output Frequency Range	f	156.250000 / 156.253906 156.257812 / 156.261718 161.132800			MHz	156.253906 MHz, +25 x10^{-6} from 156.250000 MHz 156.257812 MHz, +50 x10^{-6} from 156.250000 MHz 156.261718 MHz, +75 x10^{-6} from 156.250000 MHz
Supply Voltage	Vdd	+2.25	+2.5	+2.75	V	
		+2.97	+3.3	+3.63		
		+2.25	–	+3.63		
Operating Temperature Range	T_use	-20	–	+70	°C	Extended Commercial
		-40	–	+85		Industrial
Frequency Stability	F_stab	-10	–	+10	x10^{-6}	Inclusive of initial tolerance, operating temperature, rated power supply voltage, and load variations
		-20	–	+20		
		-25	–	+25		
		-50	–	+50		
First Year Aging	F_aging1	-2.0	–	+2.0	x10^{-6}	T_A=+25°C
10-year Aging	F_aging10	-5.0	–	+5.0		T_A=+25°C
Duty Cycle	DC	45	–	55	%	
Input Voltage Low	V_{IL}	–	–	Vdd x 0.3	V	Pin 1, OE or $\overline{ST}$
Input Voltage High	V_{IH}	Vdd x 0.7	–	–	V	Pin 1, OE or $\overline{ST}$
Start-up Time	T_start	–	6.0	10	ms	Measured from the time Vdd reaches its rated minimum value.
Resume Time	T_resume	–	6.0	10	ms	In Standby mode, measured from the time $\overline{ST}$ pin crosses 50% threshold.
LVPECL, DC and AC Characteristics						
Current Consumption	Idd	–	+61	+69	mA	Excluding Load Termination Current, Vdd = +3.3V or +2.5V
OE Disable Supply Current	I_oe	–	–	+35	mA	OE = Low
Standby Current	I_std	–	–	+100	µA	$\overline{ST}$ = Low, for all Vdds
Output Voltage Low	V_{OL}	Vdd - 1.9	–	Vdd - 1.5	V	
Output Voltage High	V_{OH}	Vdd - 1.1	–	Vdd - 0.7	V	
Rise/Fall Time	Tr,Tf	–	300	500	ps	20% to 80%
OE Enable/Disable Time	T_oe	–	–	120	ns	f = 156.25 MHz - For other frequencies, T_oe = 100ns + 3 period
RMS Phase Jitter (random)	T_phj	–	0.25	0.3	ps	IEEE802.3-2005 10GbE jitter measurement specifications
LVDS, DC and AC Characteristics						
Current Consumption	Idd	–	+47	+55	mA	Excluding Load Termination Current, Vdd = +3.3V or +2.5V
OE Disable Supply Current	I_oe	–	–	+35	mA	OE = Low
Standby Current	I_std	–	–	+100	µA	$\overline{ST}$ = Low, for all Vdds
Rise/Fall Time	Tr,Tf	–	495	600	ps	20% to 80%
Differential Output Voltage	V_{OD}	+250	+350	+450	mV	
V_{OD} Magnitude Change	ΔV_{OD}	–	–	+50	mV	
Offset Voltage	V_{OS}	+1.125	+1.2	+1.375	V	
V_{OS} Magnitude Change	ΔV_{OS}	–	–	+50	mV	
OE Enable/Disable Time	T_oe	–	–	115	ns	f = 156.25 MHz. For other frequencies, T_oe = 100 ns + 3 periods
RMS Phase Jitter (random)	T_phj	–	0.25	0.3	ps	IEEE802.3-2005 10GbE jitter measurement specifications

Consult our sales representative for other specifications.

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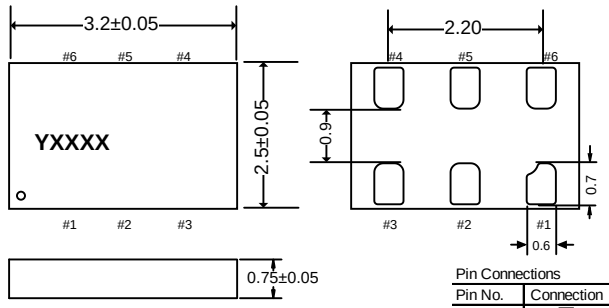
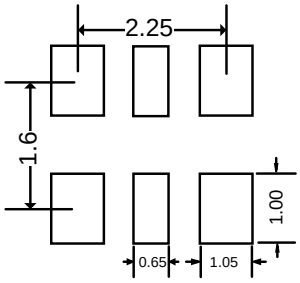
■Dimensions and Patterns

Package Size – Dimensions (Unit: mm)[1]	Recommended Land Pattern (Unit: mm)[2]

3.2 x 2.5x 0.75 mm

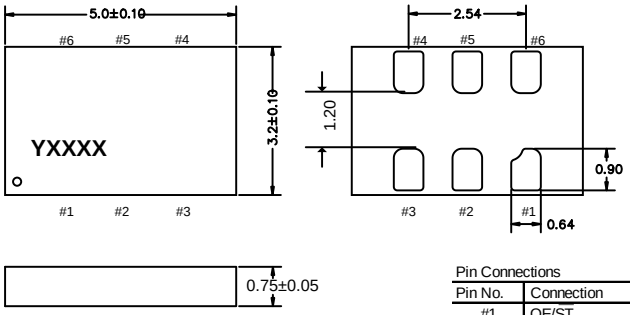


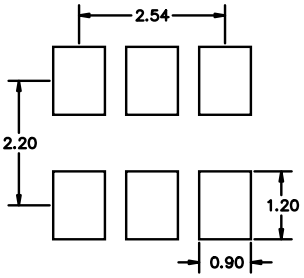


Pin Connections

Pin No.	Connection
#1	OE/ST
#2	NC
#3	GND
#4	Output+
#5	Output-
#6	Vdd

5.0 x 3.2 x 0.75 mm

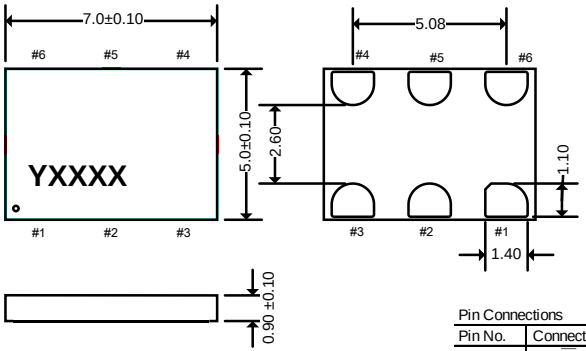


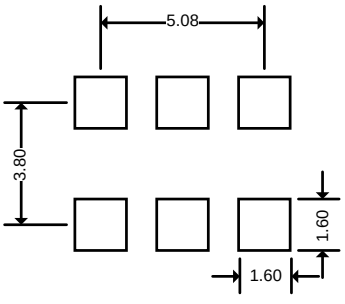


Pin Connections

Pin No.	Connection
#1	OE/ST
#2	NC
#3	GND
#4	Output+
#5	Output-
#6	Vdd

7.0 x 5.0x 0.90 mm





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#1	OE/ST
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#3	GND
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#5	Output-
#6	Vdd

Notes:

1. Top marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
2. A capacitor of value 0.1 µF between Vdd and GND is recommended.